LGP 21

Maintenance Manual

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SECTION I

INTRODUCTION

1.1 PURPOSE OF MANUAL

This manuscript is issued as the basic source of technical information on the LGP-21 Electronic Computer System. Descriptive data, explanations of the theory of operation, and maintenance instructions for this system are provided herein.

This manuscript is designed as a technical service aid for personnel who have had some previous training in computer fundamentals and theory. Technical and maintenance information is covered in sufficient detail to enable qualified personnel complete service coverage of this equipment.

1.2 TYPE OF EQUIPMENT

The LGP-21 is a general purpose, solid-state, internally programmed, electronic digital computer designed to provide reliable computation and data reduction. It is a single address, serial, binary calculating device with a magnetic disc type memory device.

1.3 DESCRIPTION OF SYSTEM

The LGP-21 System is made up of the LGP-21 Computer and a modified Flexowriter as the primary input-output device. A digital display unit and a Tally Paper-Tape Punch and Paper-Tape Reader are available as optional equipment. Additional input-output equipment may be available at a later date.

1.3.1 Physical Specifications - Computer Characteristics

Computer Type	Digital, General Purpose
Number Base	Binary
Program Type	Internally Stored
Instruction Type	Single Address
Operation	Serial
Number of Commands	23
Memory Type	Disc
Memory Capacity	4096 words
Word Size	30 Bits plus sign
Number of Breakpoints	4
Disc Speed	1180 rpm
Average Access Time	25 ms.
Minimum Latency Access Time	0.78 ms.
Clock Frequency	80 Kc.

Command Execution Times (excluding Access Time)	0. 39 ms. for all Commands except M multiply, N multiply, and Divide. M multiply: 25. 8 ms. N multiply: 25 ms. Divide: 26 ms.
Input/Output Format	Decimal, Alphanumeric, and Hexadecimal
Input/Output Capabilities	<u>Device</u> — <u>Maximum Rate/Second</u> Flexowriter — 10 Characters Paper-Tape Punch — 60 Characters Paper-Tape Reader — 60 Characters
Physical Dimensions	Height: 12 inches Width: 31 inches Depth: 19 inches
Weight	100 pounds (approximately)
Power Requirements	300 Watts (approx.) excluding I/O 117 Volts AC, single phase, 60 cps.

1. 3. 2 General Characteristics

The LGP-21 Computer contains arithmetic and control registers and internal memory for the system. Operation of the computer is under control of an internally stored program which consists of numerically coded instructions along with the data upon which operations are to be performed. The operator is provided with a means to ascertain the internal state of operation and to interrupt or alter the program by means of switches located on the control panel.

Word Structure--Within the internally stored programs the instructions and data are stored interchangeably in units of computer memory called WORDS. Each word contains 31 bits (binary digits) numbered from zero through 30 (left to right), as shown in Figure 1-1. The most significant bit indicates the algebraic sign (±) of the word, while the remaining 30 bits either indicate magnitude in the case of a data word or define an instruction and an operand address in the case of an instruction word.

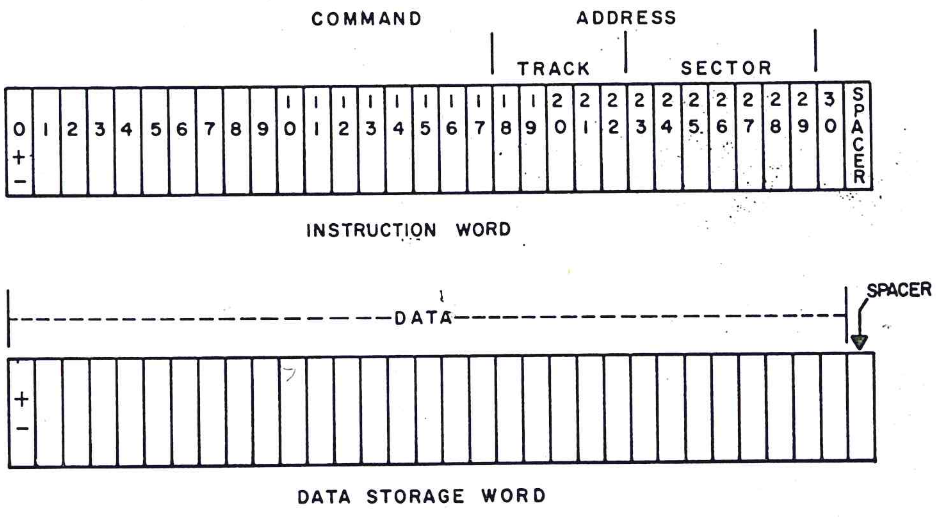

FIGURE 1-1 WORD STRUCTURE

The computer uses a single-address instruction word, with each instruction made up of two parts: The command or numerical code for the specific operation to be performed (four binary digits and the sign bit); and the address or location in memory to be referred to during the execution of the command (twelve binary digits).

The address portion of the instruction word consists of two parts which indicate the track and sector location in memory to be referred to during execution of the command. The bit locations of the track and sector are indicated in Figure 1-1.

As indicated in Figure 1-1, the computer employs a single address instruction word so that normal operation is serial. This means the instructions are executed in the same sequence in which they are stored in memory; however, some commands enable interruption of the sequential operation. These are discussed along with all other commands in Section II.

Arithmetic operations, which are performed internally using the binary number system, employ the fixed-point concept. That is, all numbers are treated as having the decimal point fixed between the sign bit and the most significant magnitude bit. Therefore, all numbers are fractional; i.e. $1>x\geq-1$.

Registers-- There are four registers in the LGP-21 Computer, which are recirculating lines used to provide a short access-time memory. These are the Control Register (C), Instruction Register (R), Accumulator (A), and the Extended Accumulator (A*). Each consists of a recording head with a read head following it (in the sense of disc rotation.) The time interval between the recording of a digit in the recirculating register and its availability from the read head (after amplification and reshaping) is one word-time, with the exception of A* which is two word-times plus one bit. This signal, with the exception of A*, is sent back to the record head which precedes it rotationally, continuously circulating each word. Provision is made for the modification of the contents of these registers.

The functions of the various registers are as follows:

The Control Register (C)	Commonly called the "Counter," holds the address of the next instruction to be executed.
The Instruction Register (R)	Contains the instruction being executed, and during multiplication or division holds one operand.
The Accumulator (A)	Retains the number resulting from the execution of the last arithmetic operation or from certain logical operations.
The Extended Accumulator (A*)	is a two word plus one bit shifting register used only during multiplication and division.

1.4 LGP-21 COMPUTER

The LGP-21 Computer (Figure 1-2) consists of four basic sections: the power supply (1), logic section (2), memory section (3), and the control panel (4). A digital display unit is optional. Each section is discussed on the following pages.

1.4.1 Power Supply

The power supply section contains a stepdown transformer, three full wave rectifiers, filter capacitors, a delay relay, a start relay for the disc motor, and a running time meter. The transformer has a multiple tap primary so that correct DC voltages may be obtained if the average AC line voltage is between 107 and 127 volts. The DC output voltages are -20 volts at 7 amps max, -15 volts at 0.75 amps, max, and +15 volts at 0.5 amps. max. The Delay Relay delays the -20 volts, -20d, to the memory section to allow the disc to reach operating speed and prevent loss of stored information.

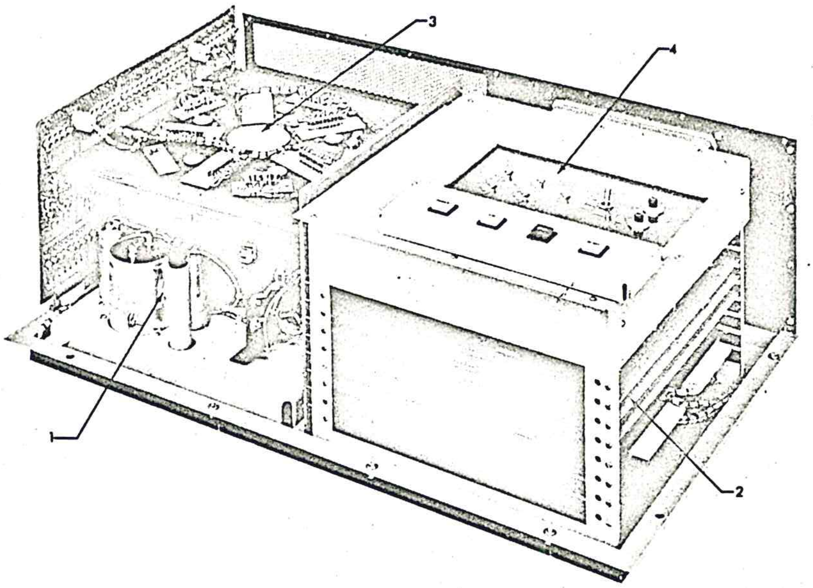

FIGURE 1-2 LGP-21 COMPUTER SECTIONS

1. 4. 2 Logic Section

The logic section consists of printed circuit cards, with the necessary circuitry for signal and power distribution, along with printed circuit connectors and the distribution board, into which the following logic cards are inserted:

P and Q Register Card
Arithmetic Card
Phase Control Card
I/O Card (Flex-Tally)

The printed circuit connectors are wired identically, and the printed circuits are designed so that the cards are completely interchangeable in the distribution board. Therefore, the location of the cards in the distribution board is not critical.

The distribution board also holds two printed circuit relays which control indicators on the control panel.

1. 4. 3 Memory Section

The memory section (Figure 1-3) consists of a magnetic disc (1), along with the associated magnetic read-write heads (2) and electronic circuitry (3), and serves as the information storage (main memory) for the computer. The main memory has a capacity of 4096 words. Thirty-two tracks (00 through 31) circumscribe the magnetized surface of the disc; and one hundred twenty-eight sectors (000 through 127) are located circumferentially within each track in an interlace pattern. Each track is provided with its own read-write head. Since the positions of the binary digits occur circumferentially on the disc, they successively come into position under the heads as the disc rotates for serial reading and/or recording. Timing pulses, derived from permanently recorded tracks on the disc in conjunction with the electronic circuitry, synchronize the operation of the computer and positively locate specific word and digit positions on the disc.

Any particular word position in main memory may be identified by specifying the track and the sector in which it is located. The address of word positions in memory are designated by two distinct sets of numbers, 00-000 through 31-127. The translation of an address so designated into the coordinates of track and sector is accomplished electronically.

Located radially on a mounting plate above the surface of the disc are five blocks of nine heads each. The area of the disc directly under these heads, along with the heads and the associated circuitry, form the main memory, timing tracks (S1, S2, S3) and the clock track.

NOTE: Only 36 heads are used: 32 for main memory, 3 for timing tracks, and 1 for the clock track. The remaining heads are spares.

The mounting plate also holds four special head-mounting blocks, which provide the A, C, R and A* recirculating registers. There are two heads on each block, one read head and one record head. The A, C and R registers are adjusted to provide registers one word-time long, while the A* register is adjusted to provide a register two words and one bit-time long.

See Sections III and IV for more detailed discussions of the memory section, head adjustments, and head replacement.

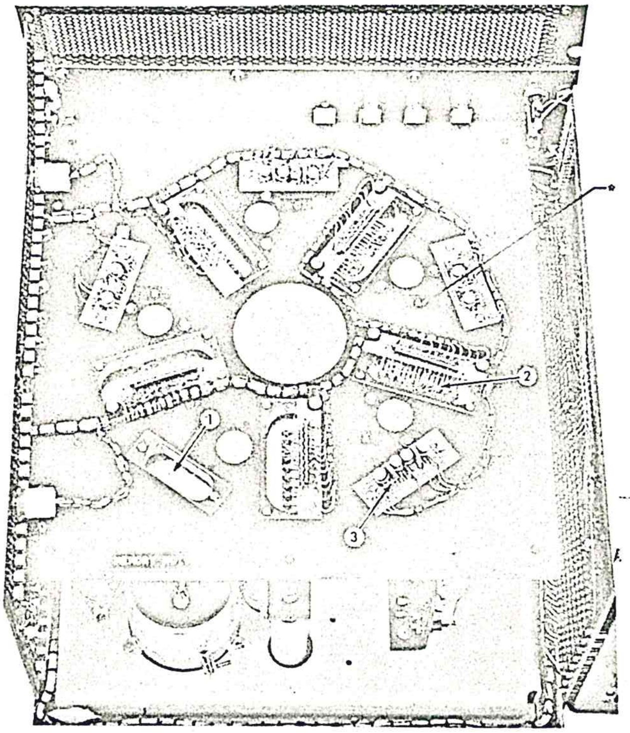

FIGURE 1-3 MEMORY SECTION

1.4.4 Control Panel

The control panel is located on the top, right, front corner of the computer. It contains eleven switches necessary to provide operator control of the computer, along with four indicator lights.

As seen in Figure 1-4, the control switches are separated into two groupings. The upper group contains eight of the control switches, and has a small door which covers them. These switches are BREAKPOINT 4, 8, 16, 32, TRANSFER CONTROL, MODE, FILL CLEAR, and EXECUTE. The FILL CLEAR and EXECUTE switches are momentary push button type, while the other six are toggle-type. The lower group contains the POWER, I/O, and START switches (each of which contains an indicator light) and a STOP indicator light.

All of the switches, except POWER, are connected to the distribution board to form logic inputs. Printed circuit relays, located on the distribution board, control the START, STOP, and I/O indicator lights on the control panel. The POWER switch applies A C directly to the power supply transformer and the memory disc motor.

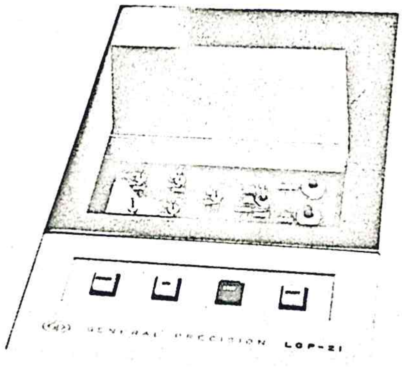

FIGURE 1-4 CONTROL PANEL

1.4.5 Rear Panel

The following items are located on the rear panel (Figure 1-5):

(1) Fan Filter and Cover
(2) RECORD ENABLE switch
(3) INTERLOCK Circuit Breaker
(4) Fuse 3 - AC Power (Computer)
(5) Fuse 2 - AC Power (Input-Output)
(6) Fuse 1 - AC Power (Accessory Connectors)
(7) Accessory Connector
(8) Input Connector
(9) Accessory Connector
(10) Display Connector
(11) Flexowriter Connector
(12) Tally Reader Connector
(13) Tally Punch Connector

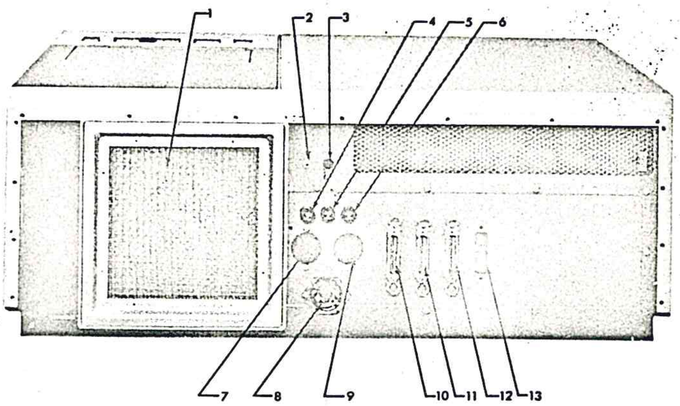

FIGURE 1-5 REAR PANEL

The fan filter and cover snaps off and on the rear cover. Pry at the top of the filter cover to remove it. The filter is a permanent type, which can be cleaned by tapping it over a waste receptical to remove loose dirt, and then brushing it clean. A schedule for cleaning this filter should be determined for each account. The thermistor will cut-off machine power if the air flow is stopped and the computer heats excessively.

1.5 INPUT/OUTPUT DEVICES

The Input/Output devices (Figure 1-6) available for the LGP-21 Computer include the Flexowriter, the Tally Paper-Tape Reader, and the Tally Paper-Tape Punch. A Digital Display Unit is also available.

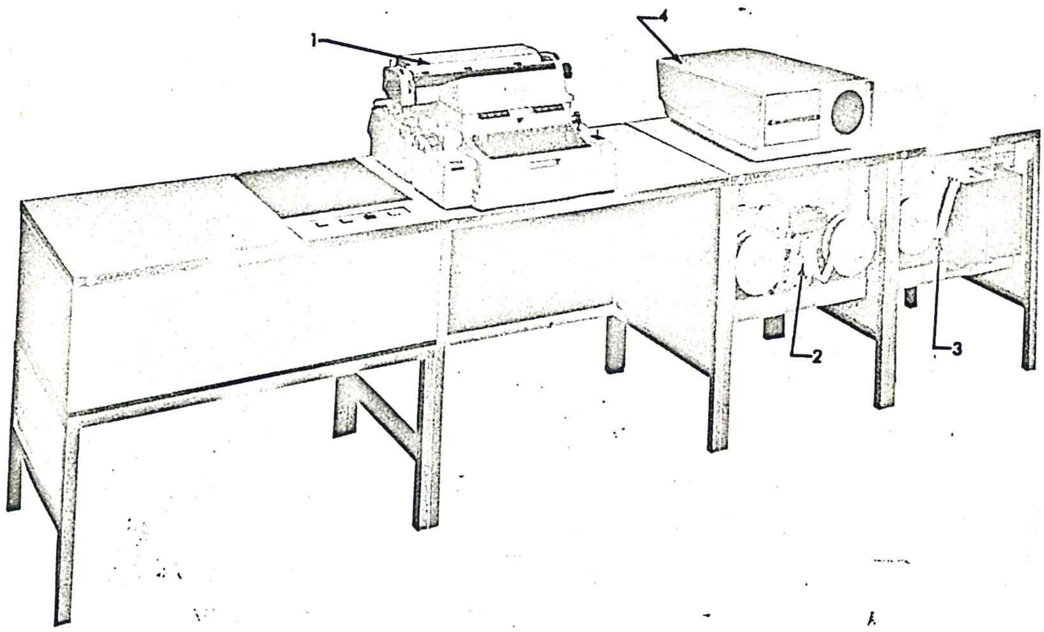

FIGURE 1-6 LGP-21 COMPUTER SYSTEM

The primary input-output device is a Flexowriter (1) that has been modified to operate with codes that are compatible with the LGP-21 Computer. Input information may be either manually initiated via the keyboard or read from perforated paper tape by the mechanical reader located on the side of the Flexowriter. Output from the computer may be either printed on hard copy or simultaneously printed and punched into paper tape. The flexowriter has a maximum operating speed of 10 characters per second.

The optional Tally Tape Reader (2) is a self-contained bi-directional, asynchronous device for reading any standard perforated paper tape. Tapes having five to eight levels of information may be interchanged and read without reader adjustment. The reading rate is a maximum of 60 characters per second.

The optional Tally Tape Perforator (3) is a self-contained, electrically operated, high speed unit capable of perforating paper tape of varying width from five to eight channels at rates up to 60 characters per second. The unit is asynchronous and can be operated at any speed below the maximum, since each character is initiated by a separate, independent pulse.

The optional Digital Display Unit (4) is a self-contained unit which will plug into the display connector on the rear panel of the computer. The oscilloscope will display simultaneously in binary form the contents of the three recirculating registers with the digit, command, and address locations marked in a graduated bezel. The manual controls for the positioning of the display are located to the left of the scope face (under a hinged cover). All the scope sweep and control circuits are contained within this unit.

Section 2

Operation

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SECTION II

OPERATION

2.1 COMMAND FUNCTIONS

Internal control of program execution is provided by instruction words. These words contain a command, which defines in binary the type of operation to be executed. There are sixteen basic commands for the LGP-21 (the composition of certain instruction words determine the specific action of some commands, effectively expanding the number of possible operations to twenty-three). These commands are represented numerically by the decimal numbers 00 through 15 and mnemonically by letters having corresponding binary configurations in memory. The commands may be divided into three groups: (1) arithmetic functions, (2) logical operations, and (3) input-output functions. The command functions will be discussed definitively below and logically in Section III.

2.1.1 Arithmetic Operations

The following nine commands are used to perform arithmetic operations. All use the contents of the accumulator during execution.

COMMAND	FUNCTION
01 B	Bring -- Replace the contents of the accumulator with the contents of the location specified by the operand address. The contents of memory are unaltered.
05 D	Divide* -- Divide the contents of the accumulator by the contents of the memory location specified by the operand address, retaining the quotient (rounded to 30 bits) in the accumulator. The absolute binary value of the contents of the memory location specified must be greater than the absolute binary value of the contents of the accumulator, or overflow will occur. The contents of memory are unaltered.
06 N	Multiply* -- Multiply the contents of the accumulator by the contents of the memory location specified by the operand address, retaining the least significant half of the product (30 bits) in the accumulator. The contents of memory are unaltered.
07 M	Multiply* -- Multiply the contents of the accumulator by the contents of the memory location specified by the operand address, retaining the most significant half of the product (30 bits) in the accumulator. The contents of memory are unaltered.
09 E	Extract -- Replace the contents of the accumulator with a bit by bit logical product of the accumulator and the contents of the memory location specified by the operand address. That is, when both the memory location specified and the accumulator contain a "1" bit, a "1" bit is written into the accumulator; if either memory or the accumulator or both memory and the accumulator contain "0" bits, write a zero in the accumulator. The contents of memory are unaltered.

* When executing divide or multiply instructions, the computer retains the contents of the specified memory location in the instruction register rather than the instruction being executed.

COMMAND	FUNCTION
12 H	Hold -- Replace the contents of the memory location specified by the operand address with the contents of the accumulator. The contents of the accumulator are unaltered.
13 C	Clear -- Replace the contents of the memory location specified by the operand address with the contents of the accumulator, clearing the accumulator to zero.
14 A	Add -- Add the contents of the memory location specified by the operand address to the contents of the accumulator, retaining the sum in the accumulator. If the sum cannot be contained in the accumulator (in 30 bits, excluding the sign and spacer bits), overflow will occur.
15 S	Subtract -- Subtract the contents of the memory location specified by the operand address from the contents of the accumulator, retaining the difference in the accumulator. If the difference can not be contained in the accumulator (in 30 bits, excluding the sign and spacer bits), overflow will occur.

2.1.2 Logical Operations

The flow of program execution may be altered by the use of the following five commands (expanded to eight operations by the word construction).

COMMAND	FUNCTION
00 Z	Sense -- Depending on the contents of the track portion of the operand address, this instruction may be used to effect two distinct modes of operation: halt or conditional skip. If the operand track address is zero, a halt occurs. If the operand track address is zero and there is a 1 in the sign bit of the instruction, the computer will interrogate and reset the overflow toggle before it halts. The skip or no skip is deferred until after the halt. (See discussion below on negative Sense instruction.) If the operand track address does not equal zero, the instruction acts as a conditional skip. The operand track address in a conditional skip instruction refers to the breakpoint switches BS-4, BS-8, BS-16, and BS-32. Any combination of these switches may be interrogated with a single Sense instruction. If all the interrogated switches are ON, the next sequential instruction is executed; if any of the interrogated switches are OFF, the next instruction is skipped. A positive skip instruction will interrogate only the referenced breakpoint switches. A negative Sense instruction will interrogate the overflow toggle. Overflow is recorded in the sign position of the counter register: a 1 indicates overflow has occurred; a 0 indicates it has not. If overflow is OFF, the computer will skip the next instruction in sequence. If overflow is ON, the computer will reset the overflow bit to zero and then execute the next instruction. Overflow and any combination of breakpoint switches can be interrogated with one Sense instruction. The operand track address designates which breakpoint switches are to be interrogated. If overflow or any

referenced breakpoint switches are OFF, the next instruction will be skipped; if all are ON, the next instruction will be executed.

02 Y	Store address -- Replace only the address portion of the memory location specified by the operand address of the instruction with the address portion of the word in the accumulator. The remaining portion of the word in memory and the entire contents of the accumulator are unaltered.
03 R	Return address -- Add 1 to the address contained in the counter register and place the sum in the address portion of the word in the memory location specified by the operand address of the instruction. The remaining portion of the word in memory and the contents of the counter are unaltered.
10 U	Unconditional Transfer -- Unconditionally transfer computer control to the memory location specified by the operand address of the instruction.
11 T	Test -- This command may be used to effect two kinds of transfer: conditional and unconditional. A positive Test instruction will transfer computer control to the memory location specified by the operand address of the instruction only if the contents of the accumulator are negative; otherwise the test instruction is ignored. A negative test instruction will transfer computer control to the memory location specified by the operand address of the instruction if either the contents of the accumulator are negative or the TC switch is ON.

2.1.3 Input/Output Operations

The following two commands effect input and output (expanded to six operations by word construction.)

COMMAND	FUNCTION
04 I	Input -- This command may effect four distinct modes of operation; shift the contents of the accumulator left four bits, shift the contents of the accumulator left six bits, input in 4-bit mode, or input in 6-bit mode. Input devices are selected by the operand track address of the instruction; the sector is irrelevent. An I 0000 in hexadecimal selects the Tally reader. An I 0200, in hexadecimal selects the Flexowriter. When an unassigned track address is used, a shift occurs. A positive shift instruction designates a 6-bit shift; a negative shift instruction designates a 4-bit shift. Input mode is determined by the sign of the instruction. A negative instruction indicates 4-bit input, and a positive instruction indicates a 6-bit input.
08 P	Print -- The print command has two functions: print in 4-bit mode or print in 6-bit mode. Output devices are selected by the operand track address; the sector address is irrelevent.. A P0200 (hexadecimal) selects the flexowriter for output; P0600 (hexadecimal) selects the Tally punch. If an unassigned operand track address is used, no operation is performed, and the next instruction is executed. The Print mode is determined by the sign of the instruction. A negative instruction will output bits 0 through 3 from the accumulator as a hexadecimal character. A positive instruction will output bits 0 through 5 from the accumulator as an alphanumeric character or a typewriter control function.

2.2 COMPUTER OPERATION

The control panel (Figure 2-1) contains the switches necessary to provide operational control of the computer.

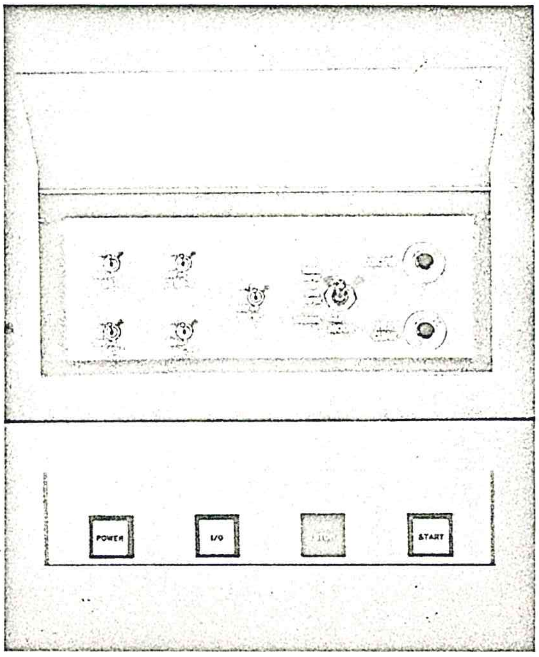

FIGURE 2-1 COMPUTER CONTROL PANEL

POWER

The POWER switch is non-latching and, when depressed, causes a relay to operate which completes the AC circuit to the power supply transformers and the memory disc motor. The POWER switch indicator lights twenty to thirty seconds after the switch is depressed, indicating that the disc has reached operating speed and the computer is ready to operate.

STOP

This red indicator light is energized when the computer enters blocked state.

START INDICATOR

The START switch indicator is lighted when the computer is not in blocked state.

I/O

The I/O switch is a momentary switch which, when depressed, will reset all input-output devices (except when in Manual Input mode) and will clear the accumulator to all zeros. If the computer is in Manual Input mode, depressing the I/O switch will not de-select the Flexowriter. The switch is lighted and operative during input and output and when the computer is in Manual Input mode.

MODE

The MODE switch is a three-position toggle switch, its three positions corresponding to the three possible modes of operation:

MANUAL INPUT - This position sets the accumulator to receive input. It also selects the Flexowriter for 4-bit input. However, no recording or erasing in memory may occur when the computer is in this mode. Characters typed on the keyboard enter the accumulator regardless of the contents of the instruction register. No instructions can be executed in Manual Input mode since the START switch is inoperative.

ONE OPERATION - With the MODE switch in this position the computer halts after the execution of each instruction. Each time the START switch is depressed, the computer will execute the instruction whose address is in the counter register and will enter blocked state. The EXECUTE switch is operative only in One Operation mode. Going from Manual Input mode to One Operation mode will de-select the typewriter.

NORMAL - In Normal mode the computer, once started, will execute internally stored serial instructions until stopped by computer control or by external control.

EXECUTE

The EXECUTE switch is a non-latching switch which is active only when the computer is in One Operation mode. Depressing EXECUTE will cause the instruction in the instruction register to be executed.

FILL CLEAR

This non-latching switch is active in both Manual and One Operation modes. Depressing the FILL CLEAR switch will cause the contents of the accumulator to be copied into the instruction register and will clear the counter register to zero.

TRANSFER CONTROL SWITCH

The TC switch is active when in the ON position. This switch furnishes the computer with additional information required for the execution of a test command as explained in Section 2. 1. 2.

BREAKPOINT SWITCHES

There are four breakpoint switches (BS-4, BS-8, BS-16, and BS-32) which are used in conjunction with the operand track address of the sense command. When the breakpoint switch corresponding to the track address of a positive Z instruction is ON, the next instruction is executed. When the switch is OFF, the next instruction is skipped.

When the breakpoint switch corresponding to the track address of a negative Z instruction is ON, or if overflow has occured, the next instruction will be executed and overflow will be reset. If there has been no overflow and all the breakpoint switches are OFF, the next instruction will be skipped.

START

This momentary switch has three possible associated reactions. They are summarized below as a function of the computer's mode of operation at the time the START switch is depressed.

1. In Manual Input mode the start switch is inoperative.

2. In One Operation mode the instruction whose address is contained in the counter register will be executed and the computer will halt. The counter register will be incremented by one unless the instruction was a transfer instruction; in which case, the counter register will contain the transfer address. The instruction register will contain the instruction just executed, except for multiply and divide instructions (see Section 2. 1. 1).

3. In Normal mode the computer will start executing instructions, starting with the instruction whose address is contained in the counter register.

RECORD ENABLE

The RECORD ENABLE switch is a toggle switch located on the back of the computer. When active it inhibits recording in (locks out) the first eight tracks of memory. Thus, a program that is to be stored permanently can be protected.

2.3 BOOTSTRAP PROCEDURE

The following sequence of operations will manually input the four instructions necessary to initiate the automatic loading of the bootstrap and subsequent Program Input 1, program J1-10.0.

1. Depress STOP READ on the typewriter.
2. Place bootstrap tape in reader.
3. Depress I/O switch on console.
4. See that all typewriter levers are UP.
5. Set MODE switch on console to MAN INPUT.
6. Depress START READ on typewriter.
7. Depress FILL CLEAR switch on console.
8. Depress START READ on typewriter.
9. Set MODE switch on console to ONE OPER.
10. Depress EXECUTE switch on console.
11. Repeat steps 5 through 9 until "normal" is typed by the computer.
12. Set MODE switch on console to NORMAL.
13. Depress START switch on console.

2.4 FLEXOWRITER CONTROLS

The Flexowriter has various control switches (Figure 2-2) located above and beside the keyboard that control input-output when it is selected by the computer. These are discussed below.

POWER ON-OFF

This switch is a toggle switch to the right of the keyboard. It turns the power to the Flexowriter ON or OFF; however, it is in series with the computer so that the Flexowriter can have power only when the computer is ON. The carriage should not be moved when the power is OFF.

START COMP

The START COMPUTE switch is operated by a momentary lever located above the keyboard. The Manual Input lever (discussed below) must be depressed, the Flexowriter must be selected for input, and the computer must be stopped on an input command. This lever is only used to indicate the end of an input (like the stop code on tape).

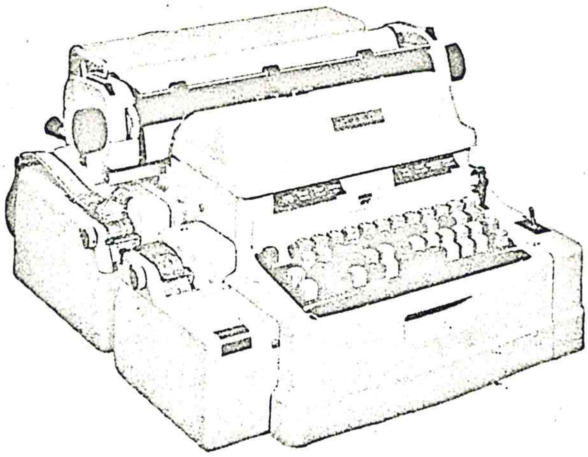

FIGURE 2-2 FLEXOWRITER CONTROLS

MANUAL INPUT

The MANUAL INPUT switch is operated by a two-position lever located above the keyboard and is unrelated to the MANUAL INPUT switch on the computer. This lever determines whether information is to enter the computer via the keyboard or the tape reader on the left side of the Flexowriter. If the lever is up, information will be read in from tape only; if down, from the keyboard only (providing the Manual Input light is lit).

CODE DELETE

The CODE DELETE switch is operated by a momentary lever located above the keyboard. It is only operative when the PUNCH ON lever (discussed below) is depressed. Each time the lever is depressed, six holes will be punched across the output tape. Thus, errors can be deleted by backing the erroneous code to the punch head and pushing the lever. When the code delete is read by the computer, it will not enter the accumulator nor will it be reproduced onto another tape. By holding down TAPE FEED and CODE DELETE at the same time, the operator can produce a series of delete codes. If, while the punch is ON, a tape interlock occurs because of a tight tape condition, depressing the CODE DELETE lever will release the typewriter.

TAPE FEED

The TAPE FEED switch is operated by a momentary lever located above the keyboard. It is only operative when the PUNCH ON lever is depressed. As long as this lever is held down, tape will feed through the punch unit and feed holes will be punched. This may be used to provide a leader at the beginning and a trailer at the end of the tape.

PUNCH ON

The PUNCH ON switch is operated by a two-position lever located above the keyboard. This lever turns ON the punch so that any characters typed from the keyboard, read from the reader device, or output by the computer will be reproduced on tape. TAPE FEED and CODE DELETE are operative only when PUNCH ON is depressed. Raising the lever turns the punch OFF.

STOP READ

Used interchangeably with START COMP.

START READ

The START READ switch is operated by a momentary lever located above the keyboard. This lever activates the reader device or, if the MANUAL INPUT lever is depressed, will turn on the Manual Input light. The reader will stop when a Conditional Stop code (') is read, providing the COND STOP lever is raised, or when the STOP READ lever, the START COMPUTE lever, or the MANUAL INPUT lever is depressed.

COND STOP

The CONDITIONAL STOP switch is operated by a two-position lever located above the keyboard. This lever is not the same as the CONDITIONAL STOP (') key which is discussed below. The COND STOP lever, when depressed, will cause the reader to ignore Conditional Stop codes. When the tape is being read into the computer, this lever must not be depressed.

COND STOP (')

In addition to the above switches, a CONDITIONAL STOP (') key has been added to the keyboard. This key punches Conditional Stop codes into the tape being produced (for subsequent input to the computer) which indicate the end of an input word.

MANUAL INPUT LIGHT

ıere is also an indicator, the Manual Input light located above the keyboard, which is lighted when the MANUAL INPUT lever on the typewriter is down and the computer is stopped on an input command. If the light is extinguished by the STOP READ switch, the computer will no longer accept input from the keyboard. If turned ON again by the START READ switch, the keyboard may again be used. When the light has been extinguished by the operator, input may be begun through the reader by raising the MANUAL INPUT switch and depressing START READ.

KEYBOARD

On the keyboard, the keys which represent the LGP-21 commands are colored differently from the rest to facilitate typing and aid in reducing mistakes.

MARGINS AND TAB STOPS

The typewriter does not have a right margin stop in the usual sense. In its place is an automatic carriage return feature. When the carriage reaches the designated point, the typewriter automatically performs a carriage return. The carriage return positioner, a clip that must be inserted manually in the carriage return rack (the rack visible from the back of the typewriter with the carriage moved to the far left), is used to determine the right margin.

osition the carriage so that the desired point is at the printing station; sight the carriage rack notch that lines up with the contact levers at the rear of the rack; move the carriage slightly, right or left, to permit insertion of the carriage return positioner in this notch without touching the contact; insert the positioner in the notch. The automatic return is reliable only if the carriage reaches the designated spot as a result of a tab. If the carriage is allowed to reach this position as the result of normal spacing, the typewriter may jam. This condition can be cleared by depressing the CARRIAGE RETURN key, but the last input or output to the computer or punch may not be correct.

Tab stops must be set manually using clips that must be inserted into the tab stop rack located behind the metal paper support. If the paper support (behind the platen) is rotated up and removed, two racks will be revealed. The lighter of these is the tab rack. The tab stops will stop the carriage at the position (shown on the paper scale at the front) corresponding to the number on the rack. The distance between notches is two character spaces.

The lower rack is the left margin rack. Every eighth notch is numbered. The margin assembly can be moved to any position, marked or not, by pressing down on the center of the assembly and sliding it along the rack. The number at the right end of the assembly indicates the position of the left margin.

TAPE INTERLOCK

Guides and interlocks on both the reader and punch devices feed the paper tape. If the tape breaks, the interlock is tripped and the device stops.

Section 3

Theory of Operations

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SECTION III

THEORY OF OPERATION

3.1 GENERAL SYSTEM LOGIC

The logic section, as seen in the System Block Diagram (Figure 3-1), forms the centeral decision element of the LGP-21 System. All arithmetic and logical functions are performed in the logic section under control of logical networks which express the internal state of main memory, the recirculating registers, the timing tracks, the arithmetic control and the input-output section.

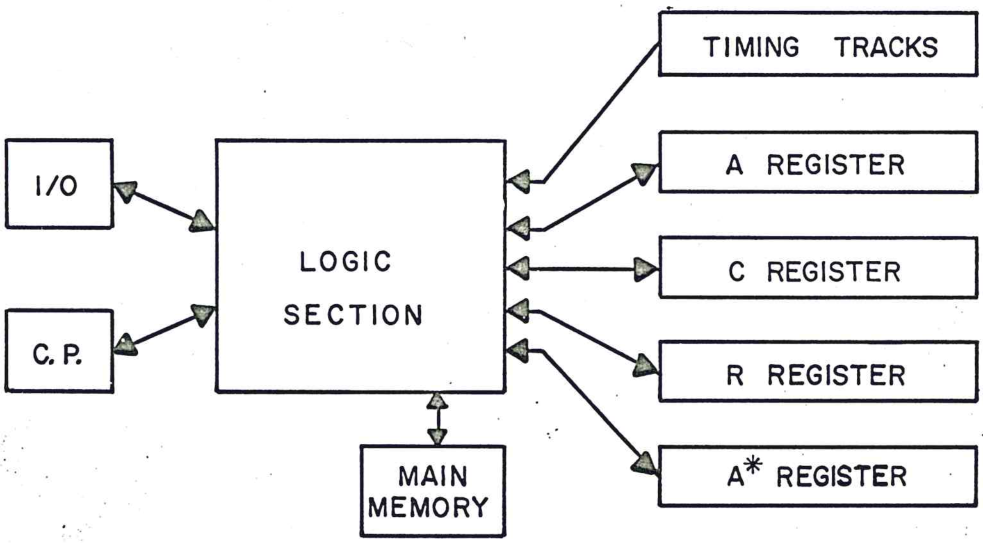


FIGURE 3-1 SYSTEM BLOCK DIAGRAM

The input or output for each bit period is a variable having one or the other of two logic voltage levels, which determine the state of the active elements. At each bit time during the execution of an instruction, the states of the active elements are examined. At the end of each bit time the states of certain active logical elements may be changed or left undisturbed, depending on the logical sequence.

The logical design of the computer consists of specified conditions in which the active elements switch state, or under which any of the other output conditions change. These conditions are conveniently described in Boolean algebra as functions of the states of the active elements and other inputs to the logical networks.

The algebraic equations used in describing the logical operations are always expressed for true voltage levels (in the area of 0 to -2 volts) corresponding to the "1" or True state of the circuit. False voltage levels (in the area of -10 to -20 volts) correspond to the "0" or False state. Each active element is identified by an algebraic character (with or without subscript).

Using a flip-flop as an example, an unmodified character denotes the signal derived from the ON side of the flip-flop, and an underscored character denotes the signal derived from the OFF side of the flip-flop. With F flip-flop on, the F output is true (0V.) and the $\underline{F}$ output is false (-20V). With F off, the F output is false (-20V) and the $\underline{F}$ output is true (0V).

The conditions required to set a flip-flop on or off are denoted by a prime (') symbol after the character, thus the equation

$$F' = \underline{F}\,G\,\underline{H} + \ldots$$

indicates: set the F flip-flop true if F is false, G is true, and H is false. The plus sign followed by three periods indicates that the F' signal may be generated by additional terms not indicated in this equation.

3.2 BASIC LOGIC CIRCUITRY

Since the logical networks determine the internal states of the active elements, an explanation of the basic logic circuit elements and their function is necessary.

The logic section is basically made up of four logical elements. They are flip-flops, nor gates, diode coupled inverters, and emitter followers. The flip-flop will be covered first.

3.2.1 Flip-Flop

The functional requirement of the flip-flop (Figure 3-2A) is to store information in the machine. It is a bi-stable device, which may be triggered from one state to the other and will maintain that state until triggered to the other state. The flip-flop will change its state only at clock time and only if the incoming logic level is steady for 1/3 clock time (about 4 μsec.) prior to the clock pulse. This is known as entrance time constant. If the input is not set for 4 μsec. prior to clock pulse, the flip-flop will not change state. This is a noise rejection feature to prevent clock jitter or line transients from making the flip-flop unreliable.

The flip-flop cannot exist in a state where both outputs are true, or false. Complementary outputs are always available. The flip-flop will never have two true inputs. Under normal conditions, one will always be false at clock time.

There are a few places in the computer with a long propagation chain, where a short entrance time constant is required. The low Zi flip-flop (Figure 3-2B) is used, since it has an entrance time constant of 1/6 clock time, or about 2 μsec.

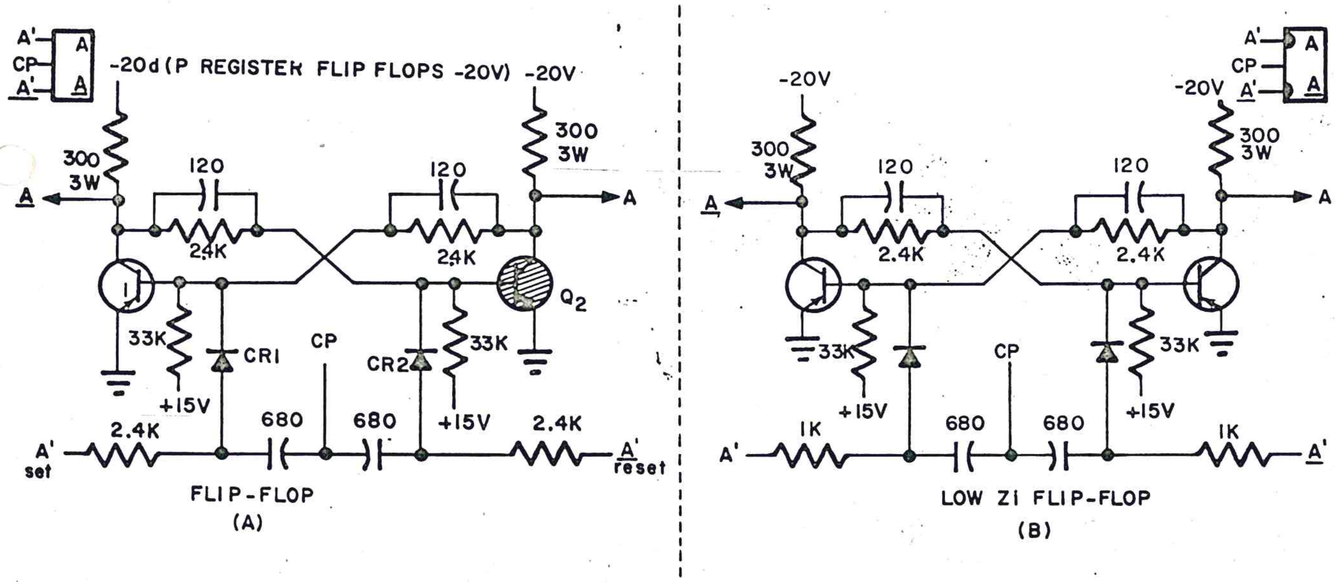


FIGURE 3-2 FLIP-FLOPS

The flip-flop, Figure 3-2A, operates in the following manner. Assuming Q2 to be conducting and the flip-flop to be in a quiescent state, the base of Q2 will be at approximately a -5 volt potential and the base of Q1 will be at approximately a +10 volt potential. This back biases CR1 and forward biases CR2. Therefore when A' goes true, the plate of CR2 will be at a 0 volt potential and its cathode will be at a -5 volt potential. Normally, the 0 volt potential would be at the base of Q2; however, because controlled forward-drop diodes are used, the base of Q2 is held at a -0.6 volts until clock time. The clock is a 4.5 microsecond, 12 volt positive-going pulse which is coupled to the base of Q2 and cuts it off. As the collector of Q2 swings toward -20 volts, the negative swing is coupled to the base of Q1, causing it to conduct and swinging its collector toward 0 volts. The positive swing is coupled to the base of Q2, holding it cut off and back biasing CR2. The diode CR1 is then forward biased, when A' comes true.

3.2.2 Nor Gate

The nor gate (Figure 3-3A) is an inverse OR gate, or an OR gate with an inverter. It has the property that when any of its input signals are false, the output signal will be true. A false output will be achieved when all the inputs are true. The input level required to change the state of a nor gate depends upon the number of input circuits and will range from -6 to -20 volts. The nor gate has a large fan in capability and a small fan out capability.

The low Zo nor gate (Figure 3-3B) is used when a nor gate output is needed in a large number of places (up to 15), but it must have less then 5 inputs.

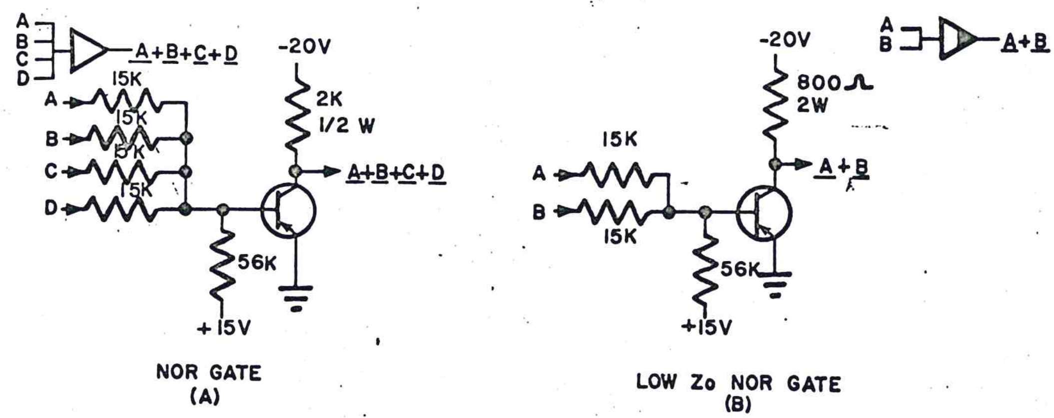


FIGURE 3-3 NOR GATES

3.2.3 Diode Coupled Inverter

The diode coupled inverter (Figure 3-4) is essentially an inverted AND gate. When any of its input signals are true, the output signal will be false. The output will be true only when all the inputs are false. The diode coupled inverter is functionally similar to the nor gate; however, the advantage of the diode coupled inverter is that it is about 10 times faster than the nor gate. It is used when a very fast propagation change is required. Its output may fan out to a maximum of 5 places.

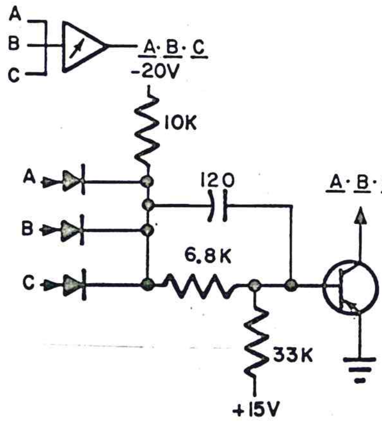


FIGURE 3-4 DIODE COUPLED INVERTER

3.2.4 Emitter Follower

The emitter follower (Figure 3-5) will follow an input signal without signal inversion at slightly less than unity gain. It is used in this machine to supply a signal to many places. The emitter follower is very fast when changing to a true state, but there is an exponential delay when changing to a false state.

NOTE: The emitter follower is the only circuit in the machine which is susceptible to damage by shorting its output to ground, so a minimum number of emitter followers are used. The emitter follower cannot directly drive a diode coupled inverter.

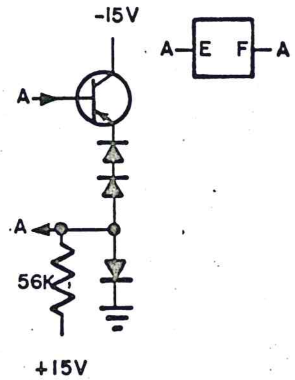


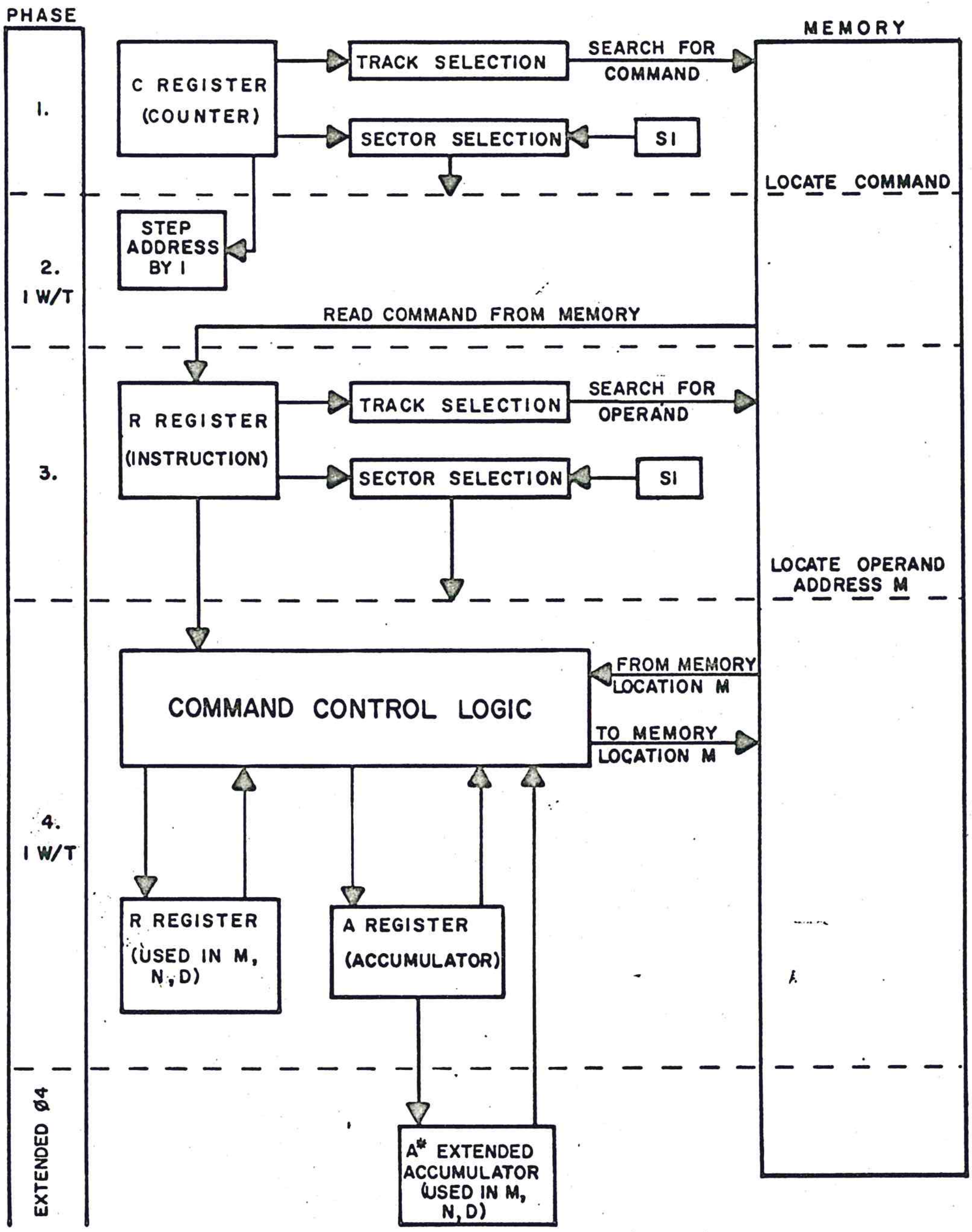
FIGURE 3-5 EMITTER FOLLOWER

3.3 TIMING

The computing cycle for the execution of each instruction is divided into four phases: phase 1 - search for instruction; phase 2 - transfer instruction from main memory to the instruction register (R) and augment the counter register (C); phase 3 - search for operand (there are instructions in which no operand search is necessary—these will be covered in command logic); phase 4 - execute the instruction.

Figure 3-6, the phase diagram, illustrates information flow thru the registers and memory.

Phases 1 and 3 each require one or more word-times for completion; Phases 2 and 4 each require one word period for all instructions, with the exception of phase 4 which is extended to 63, 65, or 66 word times for N, M, and D respectively.



Exclusive of I/O operation

FIGURE 3-6 PHASE DIAGRAM

The organization of each disc revolution into words and parts of words is accomplished by three permanently recorded timing tracks S1, S2, and S3. During each word time, the logical combination of signals from the timing tracks serve to identify the particular sector on the disc, the sign, order, and address bit time of each word. A typical word-time, showing bit times for each timing track, is shown in Figure 3-7.

A "1" identifies the periods during which the output from the playback and shaping circuits associated with each track are true. An "X" indicates a variable output corresponding to the binary number identifying the sector.

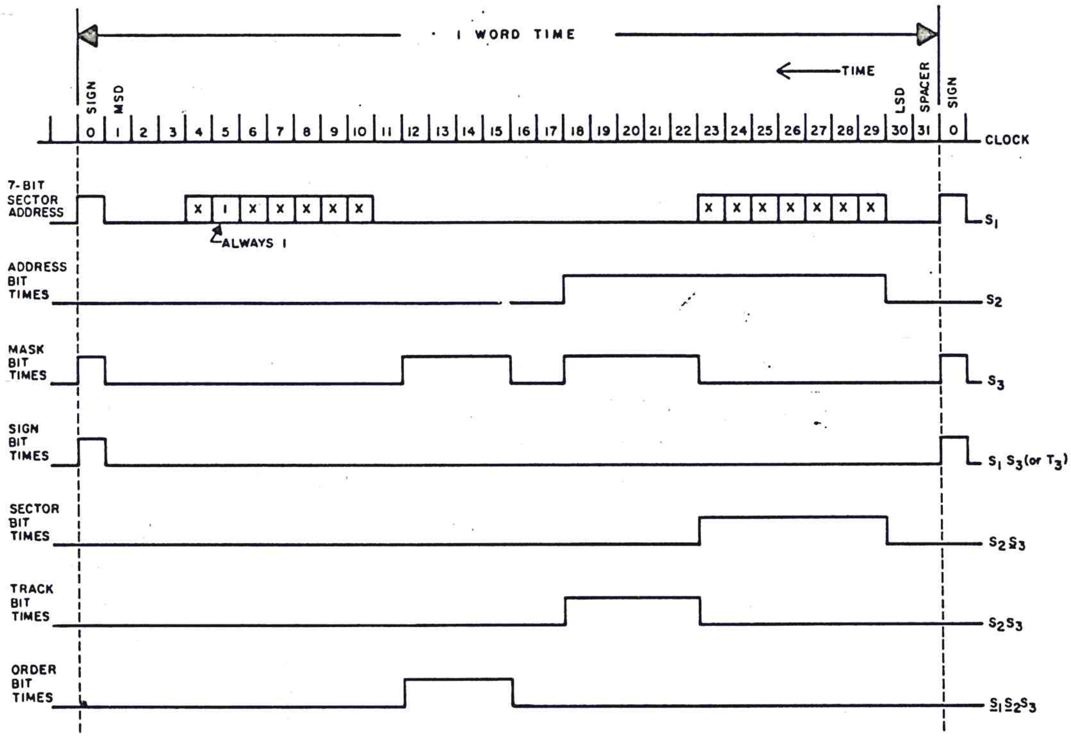


FIGURE 3-7 TIMING TRACKS

S2 marks the address bit times; $S2\underline{S}3$ marks the sector bit times; S2S3 marks the track bit times; $\underline{S}1\underline{S}2S3$ marks the order bit times; S1S3 marks the sign bit times (in the logical equations this last term is abbreviated to T3).

S1 carries the 7-bit sector address during the sector address bit time and repeats it during the 4th through 10th bit time for use in multiply and divide operations. Each word time begins and ends at the end of the sign bit time.

The sectors are addressed 00, 01, 02, etc., through 127. However, the sectors are not located in succession on the disc; that is, sector 00 and sector 01 are not adjacent but are located 18 sectors apart, resulting in an interlace pattern, part of which is shown in Table 3-1. This separation provides a 7 ms interval between instructions, assuming the instructions are performed in sequence, which permits minimum latency programming.

The four phases of each computing cycle are distinguished by the F, G, and H flip-flops. Except for the extended phase 4, the H flip-flop is always off ($\underline{H}$).

PHASE	
1	$\underline{F}\ \underline{G}\ \underline{H}$
2	$\underline{F}\ G\ \underline{H}$
3	$F\ \underline{G}\ \underline{H}$
4	$F\ G\ \underline{H}$

Phases 1 through 4 occur cyclically in the order listed. Flip-flop F is off during phases 1 and 2. F is set on at the end of phase 2, holds on during phase 3 and 4, then is set off again as phase 1 is re-entered. F is set to 1 at sign time of any phase 2 period and to 0 at sign time of any phase 4 period. Since each phase change occurs at the end of a word period, the symbol T3 is included as a factor in each equation for F and G.

$$F' = \underline{F}\ G\ \underline{H}\ T3 + \ldots$$
$$\underline{F}' = F\ G\ \underline{H}\ T3 + \ldots$$

TABLE 3-1 SECTOR NUMBERS AND ADDRESSES

Sector Number	Sector Address	Sector Number	Sector Address
1	000	19	001
2	064	20	065
3	057	21	058
4	121	22	122
5	050	23	051
6	114	24	115
7	043	25	044
8	107	26	108
9	036	27	037
10	100	28	101
11	029	29	030
12	093	30	094
13	022	31	023
14	086	32	087
15	015	33	016
16	079	34	080
17	008	35	009
18	072	36	073
		etc.	etc.

The + sign following the equation indicates that this is not the complete equation but only that part which performs the function described. Since phases 2 and 4 require only one word-time each, G may be switched off one word-time after being set on. G is switched on at the end of phase 1 or 3. The end of phase 1 or 3 is determined by the K flip-flop which will be in the on state at time T3, only for the last word-time of either of these phases, as explained below:

$$G' = \underline{G}\ \underline{H}\ K\ T3\ Q2 + \ldots$$
$$\underline{G'} = G\ \underline{H}\ T3 + \ldots$$

Q2, which indicates the absence of blocked state, is included in the G' equation. The function of Q2 in this respect is described in the section on blocked state.

3.3.1 Phase 1

In phase 1 a search is conducted for the instruction whose address is contained in the C register. For each word-time of phase 1 the bits that appear in C during the sector address time are denoted by $S2\underline{S3}$ and are compared bit by bit with the sector number being read from S1. Agreement of all seven bits indicates that the next sector is the required address and calls for the termination of phase 1. To detect this, the comparison flip-flop K is set on at the beginning of each word-time. If any bit of C and S1 disagree during time $S2\underline{S3}$, K switches off. If all bits of C and S1 agree during time $S2\underline{S3}$, K stays on through T3, ending phase 1 by allowing G to be set on.

$$K' = T3\ \underline{Faf}\ (\underline{F} + \ldots\ldots)$$

$\underline{Faf}$ means not input or output

$$\underline{K'} = \underline{G}\ \underline{H}\ S1\ S2\ \underline{S3}\ \underline{rl}\ \underline{Faf} + \underline{G}\ \underline{H}\ \underline{S1}\ S2\ \underline{S3}\ rl\ \underline{Faf} + \ldots\ldots$$
$$rl = \underline{F}\ C + \ldots$$

The $\underline{S1}\ rl + S1\ \underline{rl}$ terms will be true only if S1 and C disagree.

$S2\underline{S3}\ \underline{G}\ \underline{H}$ indicate sector time of phase 1 or 3.

To select the correct track prior to the entry into phase 2, the five bits presented by the C register during the time marked by S2S3 are copied into flip-flops P1 through P5. For this purpose six flip-flops are connected into a shifting register, the bits from C being copied into P1 and one bit time later being shifted into P2, etc. (P6 is included in this shifting register because of its use during I/O and left shift instructions.) In this manner the least significant bit of the track address ends in P5 and the most significant in P1 at the last bit period of time S2S3.

$P1' = i\ \underline{G}\ rl + \ldots$ Copy C each bit time
$\underline{P1}' = i\ \underline{G}\ \underline{rl} + \ldots$
$P2' = i\ P1 + \ldots$ Copy P1 each bit time
$\underline{P2}' = i\ \underline{P1} + \ldots$
$P3' = i\ P2 + \ldots$ Copy P2 each bit time
$\underline{P3}' = i\ \underline{P2} + \ldots$ etc.
$i = S2\ S3\ \underline{H}\ \underline{G} +$ which is track address time, phase 1 and phase 3.

3.3.2 Phase 2

In phase 2 the instruction whose address was found in phase 1 is copied from main memory into the R register. The bit readout from memory is denoted "V". During phase 2 the recirculation of the R register is inhibited, and new information is read in. At the end of phase 2 the new instruction is recirculated in R for the subsequent phase 3.

$Rw' = \underline{F}\ G\ \underline{H}\ V + R\ \underline{brc}\ (\underline{G} + \ldots)$
Where $\underline{brc}$ denotes that the FILL CLEAR switch is not activated.

In the above equation Rw' denotes the input to the record amplifier; R denotes the signal from the R register; $\underline{F}\ G$ indicates phase 2; and $\underline{G}$ indicates phases 1 and 3. The recirculation for R during phase 4 is excluded here as it is dependent on the command being executed. The C register containing the address of the instruction just found is augmented by 1 preparatory to the next phase 1. Flip-flop K is used as the complement control to augment C, and the addition is gated by S2 which identifies the address bit times. K is turned on at the beginning of each word-time as above. K is set off whenever the bit 0 occurs in the address held in the C register and remains off until the next word time.

$Cw' = \underline{F}\ G\ \underline{H}\ S2\ K\ \underline{C} + \underline{F}\ G\ \underline{H}\ S2\ \underline{K}\ C$
$\underline{K}' = G\ \underline{H}\ S2\ \underline{C}\ \underline{Faf}\ (\underline{F} + \ldots)$

The terms for the recirculation of the address of the next instruction during phases 1 and 3 are

$Cw' = \underline{brc}\ C\ \underline{G}\ S2 + \ldots$

The address of the next instruction will recirculate in C during phase 4 except during the execution of a U order.

$Cw' = \underline{brc}\ C\ F\ S2\ (\underline{Q1} + Q2 + \underline{Q3} + Q4) + \ldots$
The sum term of the Q's denotes all orders except U.

3.3.3 Phase 3

In phase 3 the search for the operand is similar to that of phase 1, differing only in that the address of the word sought is carried in the R register rather than in the C register. The K and P logic to permit this is:

$K' = T3\ \underline{Faf}\ (\underline{F} + G + R + Q1 + \underline{Q2} + Q3 + Q4)$
$\underline{K}' = S2\ \underline{S3}\ \underline{G}\ \underline{H}\ \underline{S1}\ rl\ \underline{Faf} + S2\ \underline{S3}\ \underline{G}\ \underline{H}\ S1\ \underline{rl}\ \underline{Faf} + \ldots$
$P1' = i\ \underline{G}\ rl + \ldots$
Where $rl = F\ R\ \underline{H} + \ldots$
$\underline{P1}' = i\ \underline{G}\ \underline{rl} + \ldots$
$P2' = i\ P1 + \ldots$
$\underline{P2}' = i\ \underline{P1} + \ldots$
$P3' = i\ P2 + \ldots$
$\underline{P3}' = i\ \underline{P2} + \ldots$ etc.
$i = S2\ S3\ \underline{H}\ \underline{G}\ ia + \ldots$
Where ia is true for all orders except
for the I/O and left shift commands.

rl here designates the phase in combination with $\underline{G}\ \underline{H}$ as well as the source of the bits to be copied into the P's.

In phase 3 the four order bits, which were read into the R register with the operand address in phase 2, are set into the Q flip-flops. This is accomplished in the same manner that the P flip-flops were set up, but at order time, marked by $\underline{S1}\ \underline{S2}\ S3$.

$Q1' = \alpha 11\ R + \ldots$ Copy R into Q1
$\underline{Q1}' = \alpha 11\ \underline{R} + \ldots$
$Q2' = \alpha 11\ Q1 + \ldots$ Copy Q1 into Q2
$\underline{Q2}' = \alpha 11\ \underline{Q1} + \ldots$
etc. for Q3 and Q4
$\alpha 11 = F\ \underline{G}\ \underline{H}\ \underline{S1}\ \underline{S2}\ S3\ \underline{bq}\ \underline{Faf}$

$\underline{bq}$ denotes that the MODE switch is not in the Manual Input position.
$\underline{Faf}$ is always true except for I/O commands.

The configuration of the Q flip-flops during phases 3 and 4 for each of the sixteen orders is shown in Table 3-2.

3.3.4 Phase 4

The execution of the order is accomplished in phase 4. The following equations used in the explanation of each order are only partial, including only those terms which are pertinent to the operation. The execution of all orders is primarily concerned with the operation of the accumulator or A register.

In phases 1, 2, and 3 for all orders, and in phase 4 for the orders U, T, H, Y, R, P, and Z, the A register recirculates its contents without change. The Q settings of these orders, for simplification, may be combined as one term for the recirculation of A:

$$Q1\ \underline{Q3}\ \underline{Q4} + \underline{Q2}\ (Q3 + \underline{Q4})$$

where $Q1\ \underline{Q3}\ \underline{Q4}$ includes orders P and H; $\underline{Q2}\ Q3$, the orders Y, R, U, T; and $\underline{Q2}\ \underline{Q4}$, the order Z.

The simplified equation for the recirculation of A in phases 1, 2, 3, and for the above orders is:

$$Aw' = A\ \underline{H}\ \underline{To} \left[\underline{F} + \underline{G} + Q1\ \underline{Q3}\ \underline{Q4} + \underline{Q2}\ (Q3 + \underline{Q4}) + \ldots \right] + \ldots$$

where $\underline{H}\ (\underline{F} + \underline{G})$ denotes phases 1, 2, and 3, and $\underline{To}$ denotes that the I/O button is not depressed.

For all other orders the A logic is extended. The terms for this extension are given in the explanation of each order.

TABLE 3-2 COMMANDS AND CODES FOR Q FLIP-FLOPS

COMMAND	CODE Q1	Q2	Q3	Q4
± Z-Sense	0	0	0	0
B-Bring	0	0	0	1
Y-Store Address	0	0	1	0
R-Return Address	0	0	1	1
± I-Left Shift (4 or 6-bit) or input(4 or 6-bit)	0	1	0	0
D-Divide	0	1	0	1
N-Multiply	0	1	1	0
M-Multiply	0	1	1	1
± P-Print (4 or 6-bit) or no operation	1	0	0	0
E-Extract	1	0	0	1
U-Unconditional Transfer	1	0	1	0
± T-Conditional Transfer or Test	1	0	1	1
H-Hold	1	1	0	0
C-Clear	1	1	0	1
A-Add	1	1	1	0
S-Subtract	1	1	1	1

3.4 MAGNETIC TECHNIQUES

When the disc is rotating and sufficient current is passed through the recording head, a strip the width of the core will be magnetized to saturation on the disc surface beneath the head. Reversal of the direction of current flow through the coil will reverse the polarity of the surface magnetization as shown in Figure 3-8.

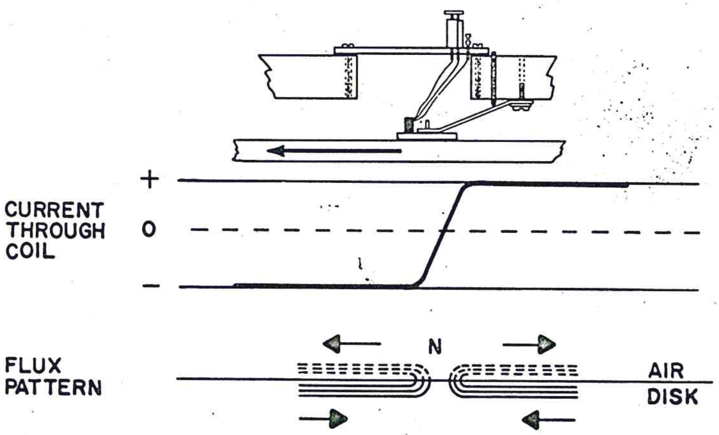


FIGURE 3-8 REVERSAL OF POLARITY

A series of reversals of the current through the recording coil on the head will produce the typical patterns shown in Figure 3-9.

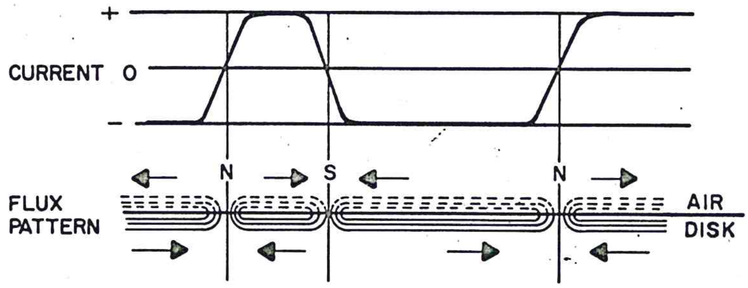


FIGURE 3-9 TYPICAL PATTERNS PRODUCED BY REVERSALS OF CURRENT

This type of recording is called "non-return to zero" because the disc surface is magnetized to saturation in one direction or the other over the entire length of the track under the record head.

If the disc surface, magnetized in the pattern just described, passes under a magnetic head which has a playback or read winding, a voltage will be induced in this coil that is proportional to the rate of change of the flux at the gap. As indicated in Figure 3-10 the flux is relatively constant except at the poles (N and S) on the disc surface. When one of these poles passes the head, a voltage pulse will be induced in the head coil the polarity of which will depend on the direction of the change of flux. If one polarity of the flux is associated arbitrarily with the recording of a binary 1 and the other polarity with 0, then the voltage pulse obtained at the read head may be converted into a form suitable for triggering a bi-stable element which will then reproduce the information previously recorded.

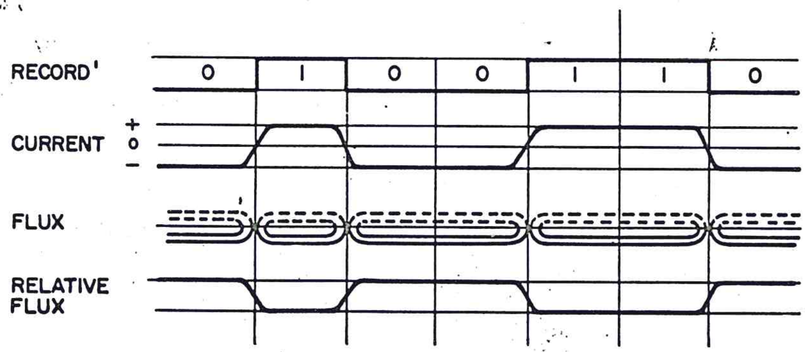


FIGURE 3-10 CHANGE OF FLUX

3.5 MEMORY

The storage of all programs and data in the LGP-21 computer is in the memory section. The memory unit consists of a rotating disc with a coating of magnetic material (hard cobalt alloy), five head blocks containing nine read-write heads each, four recirculating register head blocks, a disc drive motor and mounting plate, and the necessary associated circuitry and printed circuit cards.

The disc is approximately 10 inches in diameter. It is directly coupled to, and is driven by, a 1/40 HP motor at 1125 rpm. The disc is enclosed in a shroud, which is attached to the head mounting plate, and along with the mounting hardware forms the mechanical section of memory. See Figure 3-11.

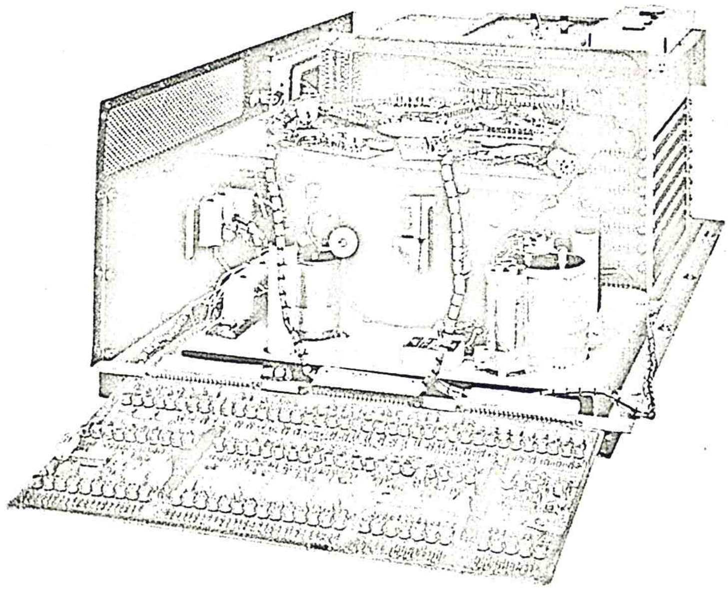


FIGURE 3-11 MAIN MEMORY

The usable area of the disc is capable of storing about 127,000 bits (4096 words of 31 bits) of main memory. In addition to which there are three permanently recorded timing tracks, a clock track, three one-word registers, one two-words-and-1-bit register, and nine spare tracks. One disc revolution is about 50 milliseconds, one word-time is about 390 microseconds, and one bit time is about 12 microseconds.

Each of the 32 main memory heads writes on a track which is approximately 0.035 inch wide. Each track is divided into 128 sectors. The tracks are numbered 00 through 31, and the sectors are numbered 000 through 127. Any word recorded on the disc may be located by specifying its track and sector numbers. For example, the word recorded on sector 124 of track 15 is addressed as 15124 in decimal, or 1WW0 in hexadecimal. Selection of main memory read/write heads is made by the write & read selection amplifier and the channel selector. For programming purposes, main memory is considered to have 64 tracks, each containing 64 sectors.

5.1 Main Memory Head Selection

Head selection is accomplished by a combination of channel selection and block selection (Figure 3-12). There are four main memory head blocks. On each main memory head block there are eight main memory heads and one spare.

A channel is selected by using the outputs of the P3, P4, and P5 flip-flops as inputs to the channel selection gate, which acts as a diode coupled inverter.

The P inputs to CR1, CR2, and CR3 are applied to the base of Q5, which has its emitter tied to a -2 volt supply. This -2 volt supply is developed across three controlled forward drop diodes (CR4, CR5, and CR6). In order to get a true, or -2 volt level, from the channel selector (Q5), all three inputs must be false, or a -20 volt level. When these inputs are false, CR1, CR2, and CR3 are back biased by .6 volt, applying -20 volts to the base of Q5, allowing Q5 to conduct. If any of the inputs are true (i.e. P3), CR1 will be forward biased, placing 0 volts at the base of Q5, thereby preventing conduction. When Q5 is conducting, it essentially becomes a short, placing a -2 volt potential at the center taps of corresponding heads in each of the four head blocks.

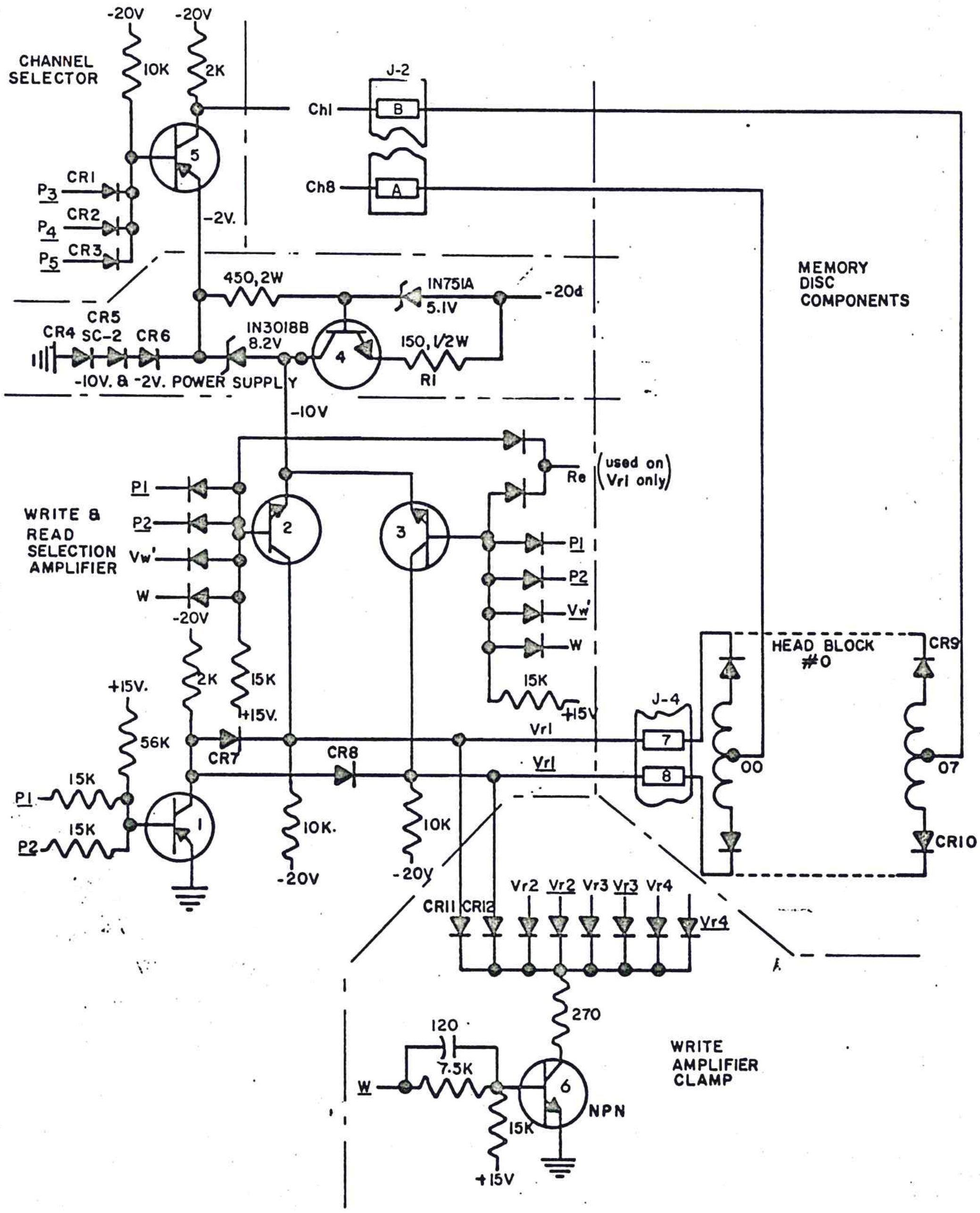


FIGURE 3-12 MAIN MEMORY HEAD SELECTION (TYPICAL CIRCUIT)

Block selection differs on read and record functions. During record, the write selection amplifier (Q2 and 3) is controlled by the appropriate output of the P1 and P2 flip-flops. The term W, which is the record term is as follows:

$$W = F\ G\ \underline{H}\ Q1\ \ Q2\ \ \underline{Q3} + F\ G\ S2\ \ \underline{Q1}\ \ \underline{Q2}\ \ Q3$$

Phase 4 of H or C Command — Phase 4 address time of Y or R Command

$$Vw' = L\ \ (\ \ A\ Q1 + A\ \underline{Q4} +$$

L: Force record 0 during spacer bit

A Q1: Copy from accumulator on H or C

A $\underline{Q4}$: Copy from accumulator on Y

$\underline{Q1}$ Q4 K $\underline{C}$ + $\underline{Q1}$ Q4 $\underline{K}$ C)
Add 1 to the contents
of the C register on
the R command

L is turned on after the spacer bit.

It may be noted that Vw' and $\underline{\text{Vw}}$'are complementary, so only one of the write amplifiers will conduct at any one time. When $\underline{\text{P1}}$ and $\underline{\text{P2}}$ are true, Q1 is cut off, placing -20 volts on the plates of CR7 and CR8. As soon as W comes true, Q2 will conduct placing -10 volts on the cathode of head diode CR9, which will forward bias it, allowing current to flow in the head winding. The path of current flow is from the -10 volt supply through Q2, CR9, and the head winding to the center tap of the head, on through Q5, CR6, CR5, and CR4 to ground. The volt supply will remain a constant -10 volts until the current through the head reaches 30 milliamps, and then will change to 0 volts. This occurs because, initially, when -20d is applied to the -10 volt and -2 volt supply, -14. 9 volts is applied to the base of Q4, and -20 volts appears momentarily at the emitter. Since the emitter is more negative than the base, Q4 will conduct dropping 8. 2 volts across the Zener Diode and 1. 8 volts across CR4, CR5, and CR6. When Q2 begins conducting and current begins to flow through the head, the -10 volts attempts to drop exponentially according to a normal voltage versus current graph of an inductor. However, when this happens, the internal resistance of the Zener Diode decreases and more current is drawn from the power supply. This increase in current causes more of an IR drop across R1, making the emitter voltage less negative. The drop across [illegible] continues to increase until the emitter voltage of Q4 goes more positive than the base. This coincides with 30 milliamps of head current. At this time Q4 cuts off and the -10 volts drops to 0 volts. As soon as this happens, -20 volts is again available at the emitter of Q4, and it again breaks into conduction. This process repeats so rapidly that 30 milliamps of head current is maintained until W goes false at which time Q6 conducts, clamping Vrl and $\underline{\text{Vrl}}$ to ground and damping the energy stored in the electromagnetic field of the head almost instantly. The effect of the -10 and -20 volt supply is such that the charging time constant to the head is linear with a fast rise time. Thus, the maximum current to the head is achieved approximately 2μsec. after the clock.

The half of the selected head which passes current determines the direction of the flux path. All other matrix selection diodes on the head block are back biased, due to the fact that all other channel voltages are false (-20V).

3. 5. 2 Write Amplifier Clamp

The write amplifier clamp, (see Figure 3-12) is energized at all times except during a record in memory function. Its primary function is performed at the end of record during a Y or R command. As $\underline{\text{W}}$ goes true, the output of the selected head is clamped at 0 volts, damping current flow in the head as quickly as possible. This has the effect of minimizing the ringing in the head due to the energy stored there from the flow of record current. The clamp circuit is CR11 and CR12 in the head block line, resistor R2, and Q6 which turns on at the end of writing, so that R2 acts as a clamping resistor across the head.

Read selection is accomplished by causing the output of the read selection amplifier (Q1) to go false. In order to accomplish this both inputs must be true. This causes the collector to go to approximately -18 volts and back biases the read selection clamp diodes CR7 and CR8, permitting the output of the head, in the selected channel, whose matrix diodes are forward biased to be fed to the memory matrix preamplifier.

3. 5. 3 Main Memory Read

Reading is accomplished by making the read selection amplifier (Q1) go false, back biasing CR7 and CR8 (Figure 3-12), and allowing the output of the head to be fed to the memory matrix preamplifier.

The memory matrix preamplifier (Figure 3-13) is a linear differential amplifier, which has a gain of approximately 290 to 1. The amplified head signal is fed to the memory matrix amplifier. The output

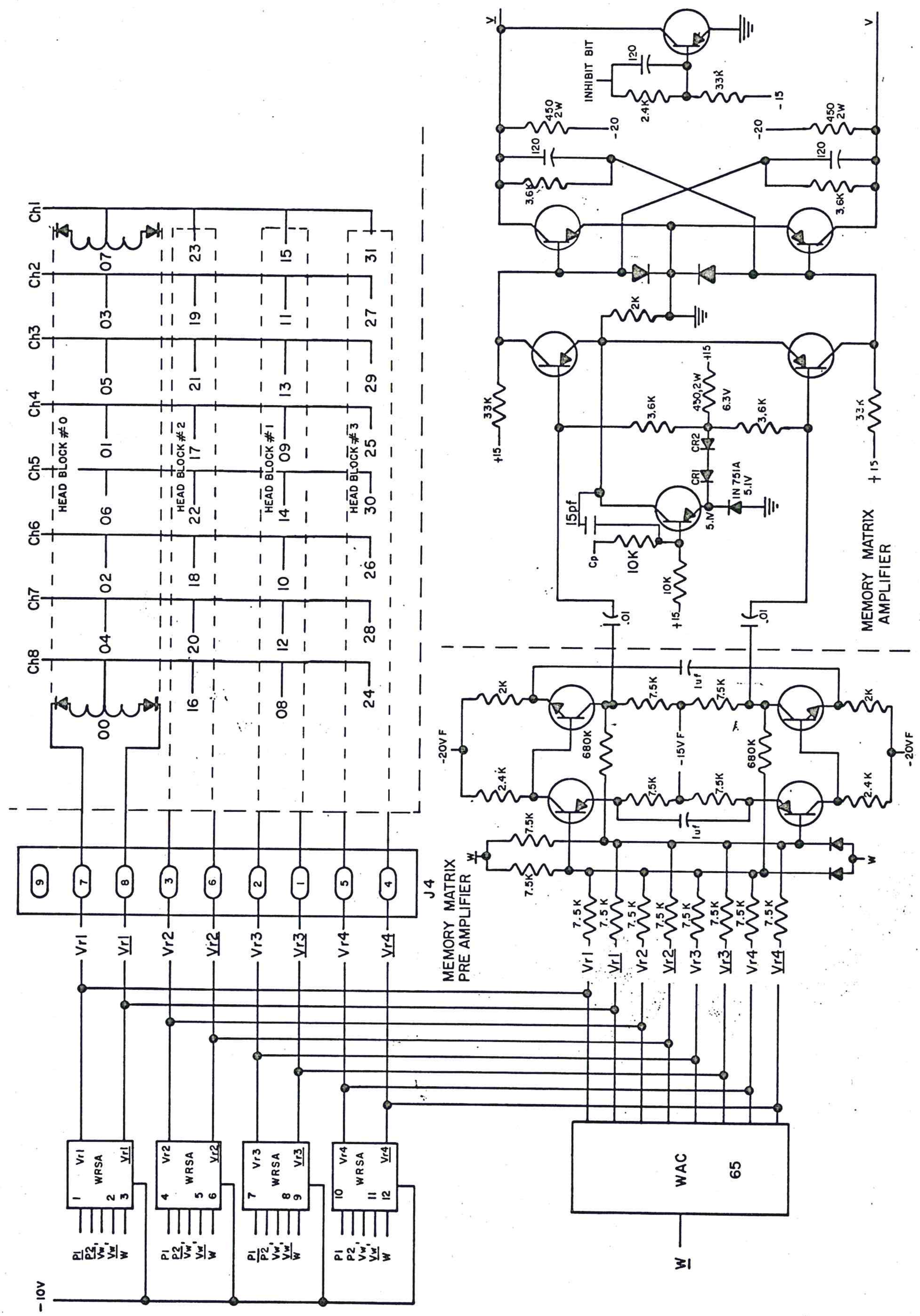


FIGURE 3-13 MAIN MEMORY READ

of the preamplifier is capacitively coupled to the bases of gating transistors Q2 and Q3 which are biased at +6.3 volts, created by the drop from ground through a 5.1 volt Zener Diode, CR1, CR2, and a 430 ohm resistor to +15 volts. Q1 is cut off, except during clock time, placing 0 volts on the emitters of Q2 and Q3. Therefore, a signal more negative than 6.3 volts is necessary to make either Q2 or Q3 conduct. This provides a noise rejection feature which makes close power supply regulation unnecessary. At clock time, a negative going pulse (Cp) of 4.5 microseconds in duration drives Q1 into conduction, placing 5.1 volts on the emitters of Q2 and Q3. This changes the effective bias of Q2 and Q3 to +1.2 volts, due to the drop across CR1 and CR2. Thus the analog signal must exceed a zero to negative peak voltage of approximately 1.6 volts before either of these gating transistors will conduct. This feature prevents base line and clock jitter and also prevents any noise of less than 1.6 volts in amplitude from gating the flip-flop indiscriminately. Since the negative swing of the linear differential amplifier is approximately 3 volts in amplitude, either Q2 or Q3 will conduct. Assuming Q2 to be conducting, the base of Q4 will be at +5.1 volts, cutting it off and driving $\underline{V}$ to approximately -20 volts. This is coupled to the base of Q5, driving it into conduction and making V equal to 0 volts. CR2 and CR3 are forward controlled drop diodes to provide additional noise rejection.

It should be noted that the collector of Q6 is connected directly to the $\underline{V}$ output. The term "Sb", which goes false during spacer bit time, causes Q6 to conduct forcing $\underline{V}$ to 0 volts. This is coupled back to the base of Q5, which forces Q5 off and Q4 on during spacer bit time.

3.5.4 Recirculating Registers

The recirculating registers, with the exception of A*, consist of a read head preceded by a write head on the same track, which are physically located 32 bit-times apart. The output of the read head is routed indirectly to the record head causing the contents of the track to be recirculated each word period. The record amplifier which is a flip-flop (Figure 3-14) causes current to flow through the write head winding to write either a 1 or a 0. Exactly 32 bit-times later the read head senses this information. The output of the read head (Figure 3-15) is amplified and shaped in the read amplifier and the data amplifier, the output of which is fed to the record amplifier by way of the logic section. The result is that, as a bit is sensed at the read head, it causes the same bit to be recorded by the record head. Thus, once each word-time each bit will be read and re-recorded.

An example of a recirculating register write circuit (Aw') is shown in Figure 3-14. The Aw' signal applied to the base of Q3 is inverted and used as the complementary input to the low Zi flip-flop. The current path necessary to write a zero is as follows: assuming Q1 to be conducting and Q2 to be cut off, the current path is from the emitter of Q2 (-18 volts) through J2 pin Y, the head, J2 pin Z, and to ground through Q1. When Aw' comes true, zero voltage is applied to the plate of CR1, and -20 volts is applied to the plate of CR2, back biasing CR2. At this time CR1 is back biased because it is a controlled forward drop diode. Therefore, Q1 is held in conduction by -.6 volt, which is developed across CR1. This condition will exist until the clock pulse (CP) is applied. The clock is a positive going 4.5 to 5.0 microsecond pulse which drives through CR1 to the base of Q1, cutting it off. Normal flip-flop action will now take place establishing a new current flow path from the collector of Q1 (-20 volts) through J2 pin Z, the head, J2 pin Y, and Q2 to ground.

An example of a recirculating register read circuit (Arh) is shown in Figure 3-15. The signal induced in the read head is amplified through a high gain, linear read amplifier. The output of the read amplifier is applied to the base of Q1 and the base of Q2 as identical signals 180 degrees out of phase. The controlled forward drop diodes, CR1 and CR2, are used to provide a positive .6 volt bias as a noise rejection feature. The amplified signal is approximately 5 volts peak to peak, and the negative swing will set either Q1 or Q2 into conduction. The conduction of Q1 or Q2 at clock time sets a low Zi flip-flop (Q3 and Q4) to obtain a logical digital signal.

The A* register is the same as all the other recirculating registers except that the read head is physically spaced 65 bit-times from the record head. This register is used only during M, N, and D functions.

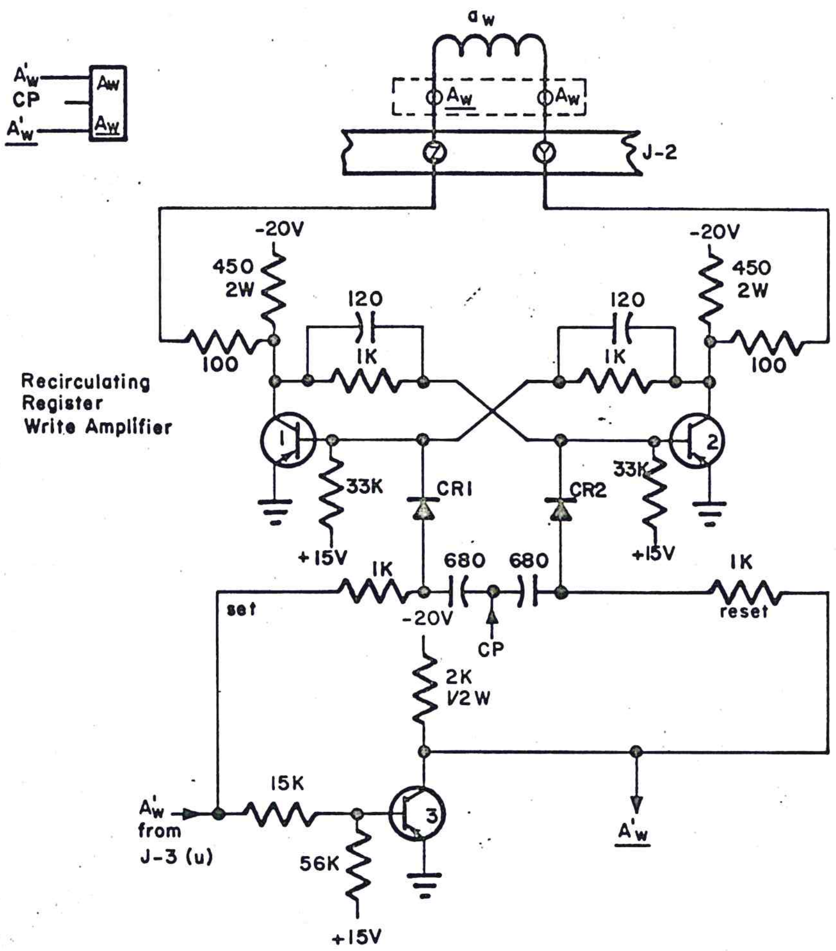


FIGURE 3-14 RECIRCULATING REGISTER WRITE CIRCUIT

3.5.5 Read Amplifier

The read amplifier, or preamplifier, is used to amplify the read head signal for the clock, S1, S2, S3 Timing Tracks, and each of the recirculating registers (C, A, R, and A*). It has an amplification factor of approximately 230. Its output is approximately a 5 volt signal whose polarity is determined by the direction of flux being read. Refer to Figure 3-16. The read amplifier is always followed by some circuit that converts its analog signal to digital information, usually a data amplifier.

3.5.6 Data Amplifier

The data amplifier, Figure 3-16, takes the analog information from the read amplifier and combines these signals with the clock to form a digital output. Its characteristic is that it takes complementary signals, if they are in the proper relationship to the clock, and sets the output to the appropriate true or false state corresponding to the level of the inputs.

The data amplifier consists of a flip-flop made up of Q3 and Q4, whose inputs are controlled by Q1 and Q2. Both Q1 and Q2 are normally not conducting due to the fact that the base is held at approximately + 0.6 volt with respect to the emitters. This 0.6 volt bias is a result of the forward drop across the silicon diodes CR1 and CR2. Therefore, in order to cause either Q1 or Q2 to conduct, a signal must occur which goes more negative than 0.6 volts. All signals below 0.6 volts will have no effect on this circuit. When a signal which is more negative than 0.6 volts is applied to the base of either Q1 or Q2, the transistors will conduct, causing the collector voltage to go to 0 volts forming a true input to one side of the flip-flop. When the clock pulse goes true, the flip-flop will be set to the state determined by which of its inputs were made true. Thus, the output of the data amplifier is a digital output which corresponds to the flux pattern on the disc.

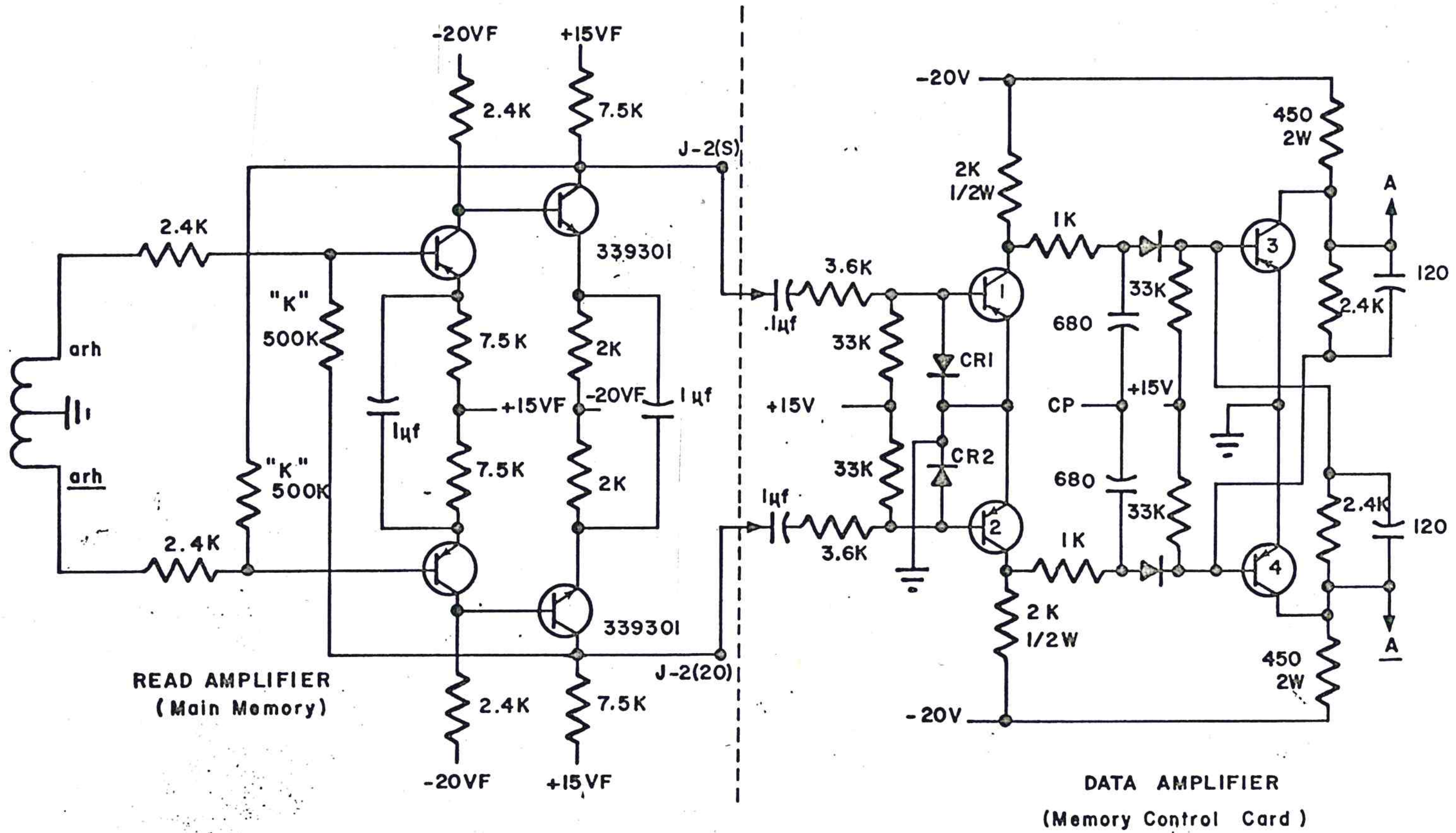


FIGURE 3-15 RECIRCULATING REGISTER READ CIRCUIT

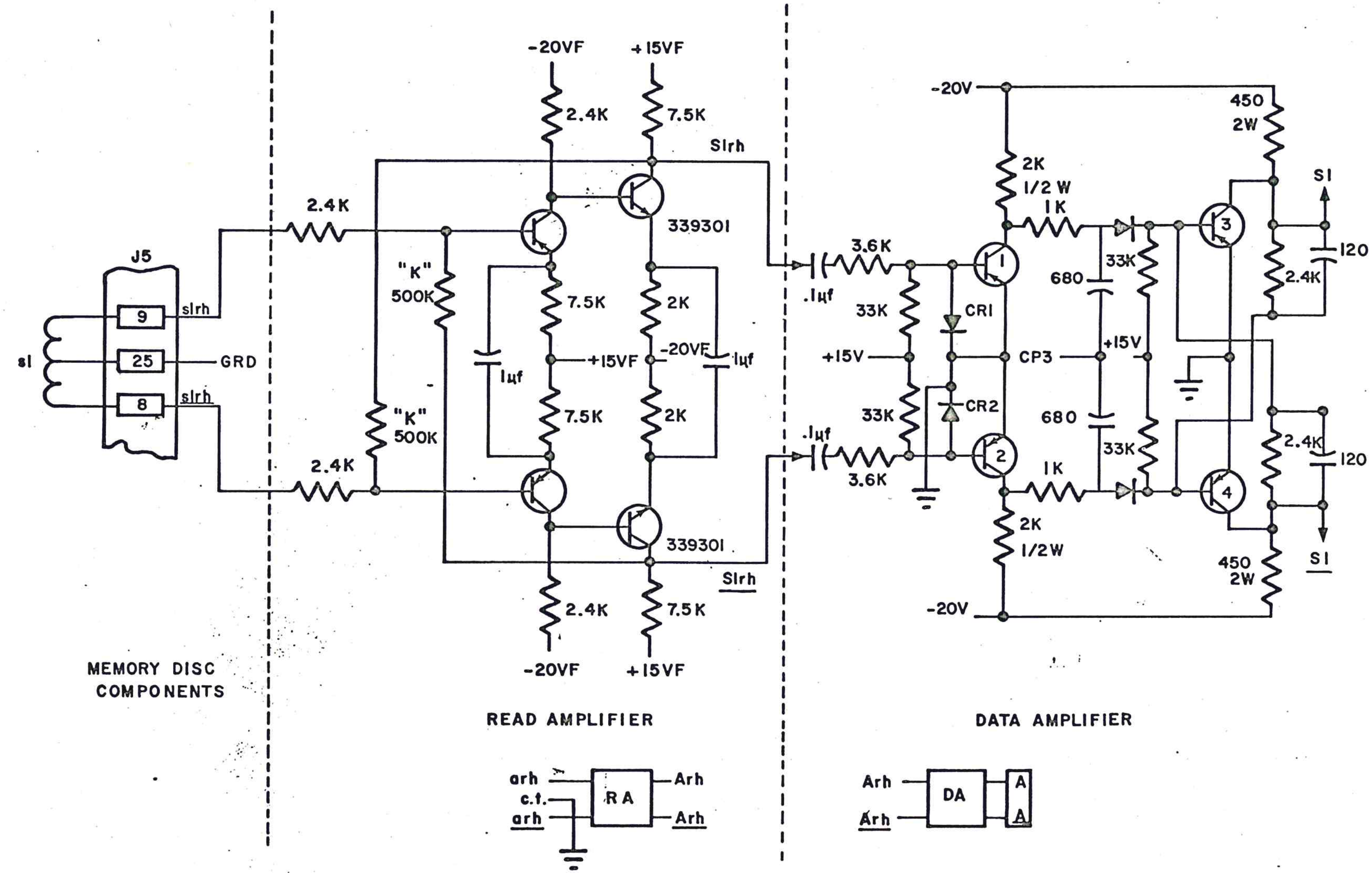


FIGURE 3-16 TIMING TRACK CIRCUIT

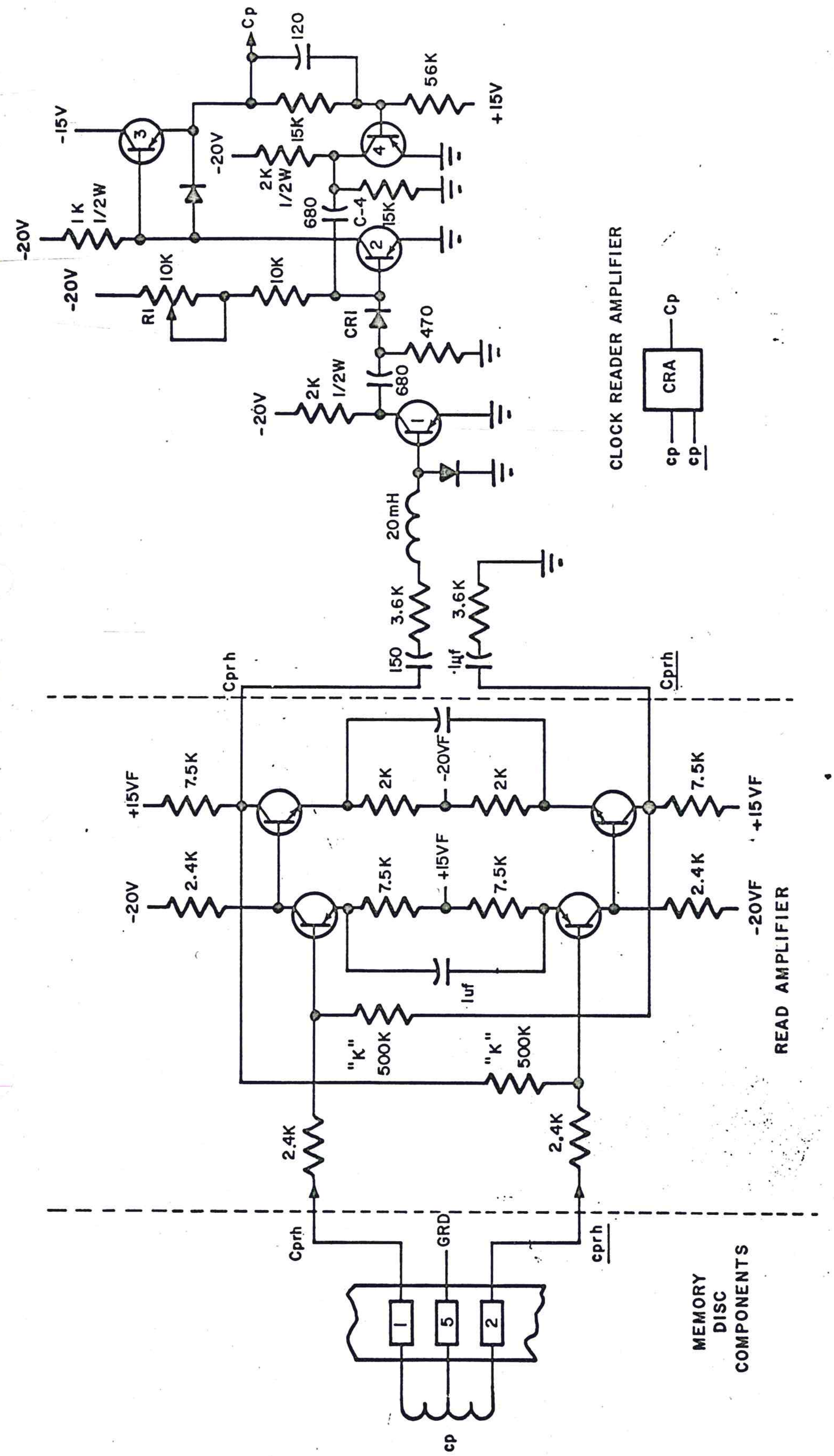


FIGURE 3-17 CLOCK CIRCUIT

3.5.7 Clock Read Amplifier

The clock read amplifier, Figure 3-17, is driven by a read amplifier which applies the analog clock signal through a differentiating network to the base of Q1, which is normally cut off. This negative signal causes Q1 to conduct, which makes its collector swing positive. This positive shift is coupled through CR1 to the base of Q2, which is normally conducting. This causes Q2 to cut off, which makes its collector swing negative. This negative swing is applied to the base of Q3, which is an emitter follower, so its emitter will also swing negative. The emitter of Q3 is coupled to the base of Q4, causing the collector of Q4 to swing positive. This positive shift is capacitively coupled back to Q2 acting as positive feedback to assist in cutting off Q2. The result of this is a negative going signal with a very sharp leading edge, which will remain negative for a period determined by the setting of R1 and C4. The output signal should be false for 4.5 microseconds and true for 7.5 microseconds. This output signal is the intermediate clock which is used directly on the main memory matrix read amplifier and as an input to the clock drivers.

3.5.8 Clock Driver

The clock driver circuit, Figure 3-18, inverts the intermediate clock to produce a signal which goes from -12 volts to 0 volts at clock time, remains there for 4.5 microseconds, and then charges exponentially to -12 volts. This output signal from the clock driver is used to energize flip-flops throughout the machine.

The intermediate clock signal will activate all the clock drivers in the machine. There is one clock driver for every 5 flip-flops and at lease one clock driver on every circuit card.

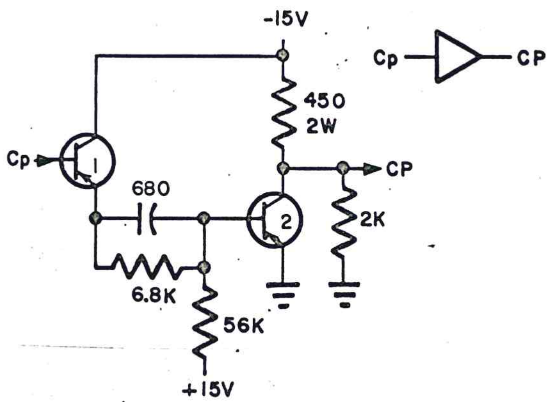


FIGURE 3-18 CLOCK DRIVER

3.6 COMMAND LOGIC.

The following command logic describes the internal logical functions of the computer as each command is being executed. Each command is defined, along with the logic for the execution of the command, and an explanation of the logic involved.

The input/output logic is covered in Section 3.8.

<u>Bring</u> ($\underline{Q1}$ $\underline{Q2}$ $\underline{Q3}$ Q4) Copy V into A. At the beginning of phase 4, inhibit the recirculation of A and substitute V in the record term. Terminate phase 4 at the end of one word-time and recirculate the new A.

$Aw' = F\ G\ \underline{H}\ \underline{Q2}\ \underline{Q3}\ Q4\ V\ (\underline{Q1} + \ldots) + \ldots$

F G $\underline{H}$ denotes phase command, $\underline{Q1}$ $\underline{Q2}$ $\underline{Q3}$ Q4 the order, and V the information from memory.

$\underline{F'} = F\ G\ \underline{H}\ T3 + \ldots$

$\underline{G'} = G\ \underline{H}\ T3 + \ldots$

Extract (Q1 $\underline{\mathrm{Q2}}$ $\underline{\mathrm{Q3}}$ Q4) Retain in A all binary digits which are in the same positions as the binary 1's of V. Set to binary 0 all digit positions in A which are in the same positions as the binary 0's in V. The operation is executed using the fundamentals of binary multiplication without the carry (re-entry multiplication). The product AV is recorded in A. Phase 4 is terminated after one word-time.

The Aw' terms for the Bring and Extract orders are combined as they differ only in the setting of Q1.

$$\mathrm{Aw'} = \mathrm{F\ G\ \underline{H}\ \underline{Q2}\ \underline{Q3}\ Q4\ V\ (\underline{Q1} + A)} + \ldots$$

If Q1 is off, copy V into A. If Q1 is on, write a 1 into A only when both V and A are true.

Add (Q1 Q2 Q3 $\underline{\mathrm{Q4}}$) Add A and V and record the sum in A. End phase 4 after one word-time.

During the add operation the flip-flop L is used to hold the binary carry digits. L is always set off at the end of each word-time except during extended phase 4.

In phase 4 for addition, L is set on following the simultaneous occurrence of 1 bits in A and V; it is set off if A and V are 0; if A and V differ, the setting of L is left unchanged, as required by the rules of binary addition. Because of operations which make use of other inputs to the adder logic, the signals A and V are formed into terms I1 and I2, respectively. The sum of A and V, taking into consideration y carries, is recorded in A by the following terms:

$$\mathrm{I1} = \mathrm{\underline{H}\ A} + \ldots$$
$$\mathrm{I2} = \mathrm{\underline{H}\ V} + \ldots$$
$$\mathrm{L'} = \beta 3\ (\alpha 5 + \ldots) + \ldots$$
$$\text{Where } \beta 3 = \underline{\mathrm{T3}} + \ldots$$
$$\alpha 5 = \mathrm{\underline{S}\ I1\ I2\ \underline{L}}$$

$\underline{\mathrm{S}}$ indicates addition

$$\underline{\mathrm{L}}' = \underline{\beta}3 + \mathrm{Q2\ (Q3} + \ldots)(\alpha 8 + \ldots)$$
$$\text{Where } \alpha 8 = \mathrm{\underline{S}\ \underline{I1}\ \underline{I2}\ L}$$
$$\underline{\beta}3 = \mathrm{T3\ (\underline{H}} + \ldots)$$

$$\mathrm{Aw'} = (\mathrm{F\ G\ Q1\ Q2\ Q3} + \ldots)(\mathrm{L\ \underline{I1}\ \underline{I2}} + \mathrm{\underline{L}\ I1\ \underline{I2}} + \mathrm{\underline{L}\ \underline{I1}\ I2} + \mathrm{L\ I1\ I2}) + \ldots$$

The inputs to $\underline{\mathrm{L}}'$ are gated by the order to allow the use of L in other operations. $\underline{\mathrm{T3}}$ inhibits the carry logic from turning L on at the end of the word period, and T3 in the $\underline{\mathrm{L}}'$ equation insures that L is set off except during extended phase 4. $\underline{\mathrm{Q4}}$ is omitted from the Aw' equation since it holds true for both addition and subtraction. The Q2 Q3 term is necessary in the $\underline{\mathrm{L}}'$ equation to inhibit carry logic from setting off luring the execution of Y, R, H, or C instructions.

Negative numbers are held in the memory and operated on as true complements and sign. A true complement is derived by subtracting each digit from the radix less 1, then adding one to the least significant digit, executing any carries required. An alternate method using the concept of the signed number system is to assign the sign digit the value 1 and to subtract the whole number from 2; i.e., the signed number representation of a negative 5 is 1.1011. Because of the form used for negative numbers, the addition process for positive and negative numbers is the same.

Subtract (Q1 Q2 Q3 Q4) Subtract V from A and retain the difference in A. Subtraction is performed by the logical process of adding V to A, determining the carries by the ones complement of A. The effect of this is taking the 1's complement of the digits in A, adding V, taking the 1's complement of the sum, and retaining the result in A. The reduction of the algebraic equations for the above operations results in:

$$\mathrm{Aw'} = (\mathrm{F\ G\ Q1\ Q2\ Q3} + \ldots)(\mathrm{L\ I1\ I2} + \mathrm{L\ \underline{I1}\ \underline{I2}} + \mathrm{\underline{L}\ I1\ \underline{I2}} + \mathrm{\underline{L}\ \underline{I1}\ I2}) + \ldots$$

$$L' = \beta 3\ (\alpha 7 + \ldots) + \ldots$$
Where $\beta 3 = \underline{T3} + \ldots$
$\alpha 7 = S\ \underline{I1}\ I2\ \underline{L} + \ldots$

$$\underline{L}' = \underline{\beta 3} + Q2\ (Q3 + \ldots)\ (\alpha 6 + \ldots)$$
Where $\underline{\beta 3} = T3\ (\underline{H} + \ldots)$
$\alpha 6 = S\ I1\ \underline{I2}\ L$

$S = \underline{H}\ Q4 + \ldots$
S denotes subtraction

The L equations represent the binary carries from the addition of V and $\underline{A}$ which is the 1's complement of A. The summing of A, V, and L (the carry) remain the same as the add operation.

Unconditional Transfer (Q1 $\underline{Q2}$ Q3 $\underline{Q4}$) Take the next instruction from the memory location specified by the address portion of the instruction. To execute this operation, the recirculation of the C register is inhibited and the R register is copied into C. Phase 4 is ended after one word-time, and the new address is recirculated in C. During the next computation cycle the instruction will be read from the memory location whose address was just copied into C from R. Because it is not necessary to perform a search for an operand in the execution of the transfer order, phase 3 is terminated after one word-time. The on term for G is

$$G' = F\ \underline{G}\ T3\ Q1\ \underline{Q2}\ Q3\ \underline{be} + \ldots$$
$$Cw' = F\ G\ \underline{H}\ \underline{T3}\ Q1\ \underline{Q2}\ Q3\ \underline{Q4}\ R + \ldots$$
Where Q1 $\underline{Q2}$ Q3 denotes the U or T order, and
$\underline{be}$ denotes not execute.

The C recirculation term is not included here as it is given in the phase 2 discussion.

Test (Q1 $\underline{Q2}$ Q3 Q4) Take the next instruction from the memory location specified in the instruction only if the number held in the accumulator is negative or if the Transfer Control switch is on and a 1 is held in the sign bit of the instruction word (negative test instruction).

Because the U and T orders differ only in the setting of Q4, the T order is executed by setting Q4 off ($\underline{Q4}$) if the above conditions are met. Since the transfer is made in phase 4, the decision to execute the transfer is made during phase 3. At sign time (T3) of phase 3, the contents of the accumulator, the Transfer Control switch, and the sign digit of the R register are examined, and Q4 is set accordingly.

$$\underline{Q4}' = Q1\ \underline{Q2}\ Q3\ T3\ A + Q1\ \underline{Q2}\ Q3\ T3\ R\ Tc + \ldots$$
Where Tc = Transfer Control switch.

Sense ($\underline{Q1}$ $\underline{Q2}$ $\underline{Q3}$ $\underline{Q4}$) Stop unconditionally, or skip the next command contingent on the breakpoint switches.

Stop: Zero track address. Enter Blocked State (see Blocked State explanation).

Conditional skip: Non-zero track number addressing the skip switches. One or more 1 bits in the track address addressing BREAKPOINT switches that are off institute the skipping operation. A non-zero track number with a corresponding BREAKPOINT switch that is on causes the next instruction in sequence to be executed.

The method by which the skip operation is accomplished is as follows: On overflow and switch sensing, the skip operation causes the computer to disregard the next instruction and execute the second sequential command. This skip operation is controlled by the state of Q1 in phase 2. If Q1 is on in phase 2, F' is inhibited and phase 1 of the following instruction is entered.

$$F' = \underline{F}\ G\ \underline{H}\ \underline{Q1}\ T3 + \ldots$$

Q1 is also set off as phase 1 is entered, allowing the normal phase sequence to continue.

$$\underline{Q1}' = G\ \underline{H}\ Q1\ \ T3 + \ldots$$

This same term sets Q1 off during phase 4, sign time for all commands when Q1 is on.

In the execution of the skip command, the states of the P flip-flops are examined in conjunction with the settings of the BREAKPOINT switches. If coincidence occurs between at least one true P state and an off BREAKPOINT switch, Q1 will be set on and a skip will be executed.

$$Q1' = G\ \underline{H}\ \underline{Q1}\ \ \underline{Q2}\ \ \underline{Q3}\ \ \underline{Q4}\ \ T3\ (P1\ \underline{Tb1} + P2\ \underline{Tb2} + P3\ \underline{Tb3} + P4\ \underline{Tb4} + \ldots) + \ldots$$

Where Tb1 through Tb4 denotes the BREAKPOINT switches.

If coincidence does not occur, Q1 will remain off and the next instruction will be taken in sequence; except, if all the P flip-flops are off, a stop will occur. (See Blocked State explanation).

Check Overflow (-$\underline{Q1}\ \ \underline{Q2}\ \ \underline{Q3}\ \ \underline{Q4}$) If an overflow condition has occurred since the last check overflow command (indicated by a 1 in the sign bit of the C register), reset the overflow bit to 0 and execute the next command in sequence. When overflow is not indicated, the next command is skipped. The -Z command will also operate in the halt mode or BREAKPOINT mode. Therefore, if only overflow sensing is desired, the instruction should be given as -Z01000 (decimal) to avoid activating the BREAKPOINT switches or the halt mode.

Q1 is turned on during overflow check when a -Z instruction is given, and no overflow has occurred.

$$Q1' = G\ \underline{H}\ T3\ \underline{Q1}\ \ \underline{Q2}\ \ \underline{Q3}\ \ \underline{Q4}\ (R\ \underline{C} + \ldots) + \ldots$$

During the execution of an add or subtract order, terms of the adder logic are examined for lack of overflow at sign time and the C register is set accordingly.

$$Cw' = F\ G\ T3\ Q1\ \ Q2\ \ Q3\ (\alpha5 + \alpha6 + \alpha7 + \alpha8) + \ldots$$

Where
$$\alpha5 = \underline{S}\ I1\ \ I2\ \underline{L}$$
$$\alpha6 = S\ I1\ \underline{I2}\ L$$
$$\alpha7 = S\ \underline{I1}\ I2\ \underline{L}$$
$$\alpha8 = \underline{S}\ \underline{I1}\ \underline{I2}\ L$$

During the execution of the divide order, an overflow will occur during the second word-time of the extended phase 4 if the numerator is larger than the denominator. Because division is accomplished by a logical process of addition and subtraction, the signs of the numerator and the remainder are used in determining whether an overflow has occurred. The sign of the partial quotient is held in A and that of the numerator in P6 during the second word-time of phase 4. The term for setting the C register on to record an overflow condition is

$$Cw' = \underline{F}\ \underline{G}\ H\ T3\ \underline{Q3}\ P1\ P6\ A + \underline{F}\ \underline{G}\ H\ T3\ Q3\ P1\ \underline{P6}\ \underline{A}$$

$\underline{F}\ \underline{G}\ H\ T3\ Q3\ P1$ denotes the sign digit of the second word-time of extended phase 4. Q3 identifies division, rather than multiplication. Because of the division process used, the sign of the numerator and that of the remainder will be different if the magnitude of the denominator exceeds that of the numerator. If not, an overflow will occur as denoted by P6 A or $\underline{P6}\ \underline{A}$.

Following a -Z command and during sign time of phase 4, recirculation of the C register is prevented, causing the overflow bit to be reset to 0.

$$Cw' = G\ \underline{S2}\ C\ \underline{brc}\ (\underline{F} + \underline{T3} + \underline{R} + Q1 + Q2 + Q3 + Q4 + \ldots) + \underline{G}\ T3\ C\ \underline{brc} + \ldots$$

The last term is added to allow normal recirculation of the overflow bit during phase 1 and phase 3. $\underline{T3}$ is added to prevent copying the sign bit from R on a U or T command.

$$Cw' = F\ G\ \underline{H}\ \underline{T3}\ Q1\ \underline{Q2}\ Q3\ \underline{Q4}\ R + \ldots$$

Blocked State   Inhibit the continuation of computation on the execution of a sense command or when in the One Operation mode.

In normal operation, setting the G flip-flop on for entering phase 2 is controlled by Q2. If Q2 is off in phase 1, G cannot be set on, and phase 1 is continued indefinitely in the blocked state.

$$G' = \underline{G}\ \underline{H}\ T3\ K\ Q2\ \underline{be}\ \underline{bs}\ Ga + \ldots$$

Where $\underline{bs}$ denotes the START COMPUTE switch is not activated, and $Ga = \underline{Faf}$

During phase 4 at sign time (T3) for orders in which Q2 is off and the order is not a sense 00, Q2 is always turned on.

$$Q2' = F\ G\ T3\ \underline{Q2}\ \underline{O1}\ (Q1 + Q3 + Q4 + P1 + P2 + P3 + P4 + P5 + P6) + \ldots$$

Where $\underline{O1}$ indicates that the machine is not in One Operation or Manual Input mode.

The Q's contained within the parentheses indicate all orders in which Q2 is off, except Sense, and the P terms indicate all but a 0 track address.

During the execution of an input order, blocked state occurs if the ONE OPERATION switch is on:

$$\underline{Q2}' = G\ T3\ \underline{Q1}\ Q2\ \underline{Q3}\ \underline{Q4}\ O1\ B1 + \ldots$$

When in the Manual Input mode, a blocked state is introduced because the ONE OPERATION switch is electrically interlocked with the MANUAL INPUT switch; i.e., O1 is true when in the Manual Input mode.

When in the One Operation mode, it is necessary to inhibit the continuation of computation after the execution of each instruction. This is accomplished by including the signal from the ONE OPERATION switch (O1) in the Q2' and $\underline{Q2}'$ equations.

If O1 is true at the end of phase 4, the setting of Q2 on is inhibited for all orders in which it is off. For all orders in which Q2 is on during phase 4 with the exceptions of multiply and divide, O1, being true, will force Q2 to be set off on entering phase 1:

$$\underline{Q2}' = G\ T3\ O1\ Q1 + \ldots$$

Here Q1 denotes the orders other than N, M, and D.

On the execution of an N, M, or D command, Q2 is set off at the end of the full operation by the same term which sets H off.

$$\underline{Q2}' = O1\ \underline{H}' + \ldots$$

To effect a release from the blocked state, the start signal (bs) sets Q2 on.

$$Q2' = \underline{F}\ \underline{G}\ \underline{H}\ bs + \ldots$$

$\underline{F}\ \underline{G}\ \underline{H}$ is included to prevent the start signal from affecting the setting of Q2 except during phase 1. The bs signal is derived from the START switch on the control panel.

Hold   (Q1 Q2 $\underline{Q3}$ $\underline{Q4}$) Record the contents of A in memory, retaining the number in the accumulator. Phase 4 is limited to one word period. Recording in main memory is gated by the term

$$W = F\ G\ \underline{H}\ Q1\ Q2\ \underline{Q3} + \ldots$$

which goes true at the beginning of phase 4 and remains true during the execution of the Hold order denoted by Q1 Q2 $\underline{Q3}$. The information to be recorded for the Hold order is denoted by the term:

$$Vw' = \underline{L}\ (Q1\ A + \ldots)$$

L is included in the record term to force-record a 0 in the spacer bit and is turned off at the end of each word-time. After the first digit time of phase 4 with W true, L is set on to allow the recording of A into memory.

$$L' = W + \ldots$$
$$\underline{L}' = T3\ (\underline{H} + \ldots) + \ldots$$

Q1 is necessary to indicate that Vw' should copy A and not C as in the R order.

A recirculates following the equations given in the phase 1 discussion.

Clear (Q1 Q2 $\underline{Q3}$ Q4) Record the contents of A in memory, clearing the contents of the accumulator to zero during phase 4. Recording in memory for the Clear order is executed in the same manner as the Hold command; however, the recirculation of the A register is inhibited leaving the contents of the register "0" at the end of phase 4. This is accomplished by forming the A recirculation term with a combination of the Q states, excluding the Clear command. The term

$$\underline{Aw}' = Q1\ \underline{Q3}\ \underline{Q4}\ Aa + \underline{Q2}\ (Q3 + \underline{Q4})\ \underline{Faf}\ Aa + \ldots$$

includes U, T, H, Y, R, P, and Z but excludes C. (See phase 1 discussion.)

Store Address ($\underline{Q1}$ $\underline{Q2}$ Q3 $\underline{Q4}$) Store only the address portion of A in memory during phase 4. The store gate term W is set true for the address portion of the word, as identified by S2, instead of for one full word-time as above. This is controlled by the order $\underline{Q1}$ $\underline{Q2}$ Q3.

$$W = F\ G\ \underline{Q1}\ \underline{Q2}\ Q3\ S2 + \ldots$$

The information to be recorded is copied from A

$$Vw' = L\ (\underline{Q4}\ A + \ldots)$$

$\underline{Q4}$ is included to indicate that Vw' is to copy A rather than C as in the R order.

L is set on before W by the term:

$$L' = F\ G\ \underline{Q2}\ + \ldots$$

This allows recording the first digit of S2 time.

Return Address (Q1 $\underline{Q2}$ Q3 Q4) Add 1 to the address held in C and record the sum in the memory.

The record gates W and L are set true as in the store address instruction. The information to be recorded is copied from C.

$$Vw' = L\ (Q1\ Q4\ K\ \underline{C} + \underline{Q1}\ Q4\ \underline{K}\ C + \ldots)$$

K, which is set on at the end of each word time, adds 1 to the least significant digit of the address portion of C by means of the terms included in Vw'. Thereafter, K acts as the carry flip-flop, being set off by the occurrence of the first 0 in C as in phase 2.

$$\underline{K}' = G\ \underline{H}\ S2\ \underline{C}\ \underline{Faf}\ (Q3 + \ldots) + \ldots$$

Multiplikator Multiplikand

Multiply N ($\underline{Q1}$ Q2 Q3 $\underline{Q4}$) Multiply A times V and retain the least significant digits of the product in A.

The process of multiplication consists of a series of additions of the multiplicand to the partial product and the shifting of the partial product for each digit of the multiplier. As multiplication continues from the first bit of the multiplier to the last, the partial product formed by each addition and shift increases from 1 word period to approximately 2, requiring a minimum of 64 word periods (2 for each bit of the multiplier) to complete the product of A and V. Phase 4 is extended by setting the flip-flop H on at the end of one word-time of the normal phase 4 when F and G are set off. Thereafter, for the next 63 word-times, the succession of arithmetic processes which form the partial product are carried out. V is copied into R during the first word-time of phase 4 to have the multiplicand available throughout the execution of the order.

$$Rw' = G\ \underline{H}\ V\ \underline{Q1}\ Q2\ \alpha 9 + \ldots$$

$$H' = F\ G\ \underline{H}\ T3\ \underline{Q1}\ Q2\ \alpha 9$$
$$\text{Where } \alpha 9 = Q3 + \ldots$$

To retain the bits of the full product the accumulator is extended to 2 word periods and 1 bit by the use of the A* register.

Note: $Aw^{*\prime} = Aw'$

During the first word period of multiplication, the two-word A* register will contain the 32 bits of the multiplier and one word of the partial product. As multiplication continues, the partial product increases to approximately two words and the multiplier decreases to zero. This is accomplished by dropping each bit of the multiplier from recirculation as it is used and shifting the remainder of the multiplier and the increased partial product to the next most significant bit position. The bits presented by the A* read head occur exactly 65 bit times after being recorded. This delay of one bit time beyond two word-times precesses or shifts the digits presented by A* one bit time for each two-word period of the multiplication process. As they are used, the bits of the multiplier are dropped off by inhibiting the recording of Aw' at the last sign bit time of each two-word period of multiplication. To accomplish this, the Aw' record equation is formed of terms which exclude the sign time of the last word of the two-word periods. To mark each of the two-word periods required for the addition of the multiplicand to the partial product, flip-flop P1 is turned off at the end of the first word period of phase 4. At the end of the next word period it is set on, then off at the end of the next word period, and so forth until the end of multiplication. For each even word period, P1 will be off; for each odd period it will be on. Excluding the first word-time of phase 4, the first word of each pair of words is marked by $\underline{P1}$ and the last by P1.

$$P1' = H\ T3\ \underline{P1} + \ldots$$
$$\underline{P1}' = G\ T3\ P1\ P1b + H\ T3\ P1 + \ldots$$
$$\text{Where } P1b = \text{I/O interlock}$$

Because of the signed-number representation used, multiplication by the first bit of the multiplier (the sign bit) is eliminated and either the multiplicand or zero is subtracted from the partial product.

The subtraction occurs in the second word period of phase 4 when the partial product (zero) is presented in lieu of A*. During the third word period, a 1 is subtracted from each bit of the multiplier if the multiplicand is negative. The effect of this is to add 1 to the least significant bit of the multiplier, which is the spacer bit. This is necessary to prevent a carry from the previous additions to the partial product from falsifying the multiplier. The carry from the addition in the even word periods, when the least significant bits of the partial product and the multiplicand are added, is extended into the odd word periods in which the remainder of the multiplier as well as the most significant bits of the partial product are read from the extended A register. (The condition in which the carry will affect the multiplier will occur only when the multiplier is positive and the multiplicand is negative.) If the multiplicand is positive, zeros will be subtracted. The two-word period in which the subtraction takes place is denoted by $\underline{F}\ \underline{G}\ H$, the even word period by $\underline{P1}$, and the odd word period by P1. The subtraction term in the normal adder logic is made true by:

$$S = \underline{F}\ H\ Q3 + \ldots$$

Where Q3 is necessary to distinguish multiplication rather than division

$\underline{F}$ H will be true only for the 2nd and 3rd word-times of multiply.

The multiplicand will be subtracted from the initial partial product in word period 2 if the sign of the multiplier is 1. During the first word period of phase 4 the sign bit of A, which is the first multiplier bit, is copied into P6 and is dropped from the A register by excluding the sign time from the Aw' equation:

$$Aw' = \underline{H}\ A\ \underline{To}\ \left[\underline{T3}\ \underline{Q1}\ Q2\ \alpha 9 + \ldots\right] + \ldots$$

Where $\alpha 9 = Q3 + \ldots$

The Q terms denote multiply only.

$$P6' = F\ G\ \underline{H}\ T3\ A\ P6a + \ldots$$
$$\underline{P6'} = F\ G\ \underline{H}\ T3\ \underline{A}\ P6a + \ldots$$

Where P6a = I/O interlock

The I2 term of the adder logic in word-time 2 is dependent on P6.

$$I2 = \underline{G}\ H\ \underline{P1}\ P6\ R$$

$\underline{P1}$ $\underline{G}$ indicates the second word period. If P6 is true, I2 will follow R; otherwise, I2 will equal zero.

The record term for word-time 2 is:

$$Aw' = (H\ \underline{P1} + \ldots)(L\ \underline{I1}\ \underline{I2} + \underline{L}\ I1\ \underline{I2} + \underline{L}\ \underline{I1}\ I2 + L\ I1\ I2)$$

Where I1 = 0 and I2 = (as above)

The adder term is the same as for normal addition or subtraction. The fact that T3 is eliminated from the equation allows the subtraction to carry through the sign time of the even word and into the odd word period.

<u>Word Period 3</u> As subtraction continues into word period 3, the Aw' equation is

$$Aw' = (H\ \underline{T3} + \ldots)\ (L\ \underline{I1}\ \underline{I2} + \underline{L}\ I1\ \underline{I2} + \underline{L}\ \underline{I1}\ I2 + L\ I1\ I2) + \ldots$$

Because P1 is true for this word-time, the term H $\underline{T3}$ will inhibit the recording of the bit which occurs at sign time. The bit which would normally be recorded at this time is the next bit of the multiplier to be used. Accordingly, it is set into P6 where it is used to control the next arithmetic operation. During this word-time the shifted multiplier is presented by A*, and 1's are subtracted from each bit position of the multiplier, if the multiplicand is negative, for the reason discussed previously. Otherwise, a zero is subtracted.

I1 follows the A* read signal. I2 will be true for the full word-time if P5 is true. P5 is set to the sign of the multiplicand during the first word period and remains in that setting for the remainder of the multiplication period.

$$P5' = G\ \underline{H}\ T3\ V\ P5a + \ldots$$
$$\underline{P5'} = G\ \underline{H}\ T3\ \underline{V}\ P5a + \ldots$$
$$P6' = H\ T3\ P1\ Q3\ A^* + \ldots \qquad \text{Copy the multiplier bit into P6}$$
$$\underline{P6'} = H\ T3\ P1\ Q3\ \underline{A^*} + \ldots$$

Q3 is included to denote multiplication.

$$I1 = A^{*}\ H\ Q3\ P1 + \ldots$$

Where Q3 P1 denotes the odd word-times of multiplication

$$I2 = H\ Q3\ P1\ \underline{F}\ P5 + \ldots$$

Where Q3 P1 $\underline{F}$ denotes the third word-time of multiplication

The carry logic to allow the subtraction and carry beyond sign time of word period 2 is

$$\begin{array}{llll} L' = & \beta 3 & (\alpha 7 + \ldots \quad) & + \ldots \\ & (\underline{T}3 + H\ Q3\ \underline{P}1) & (S\ \underline{I}1\ I2\ \underline{L} + \ldots) & + \ldots \end{array}$$

$$\begin{array}{llll} \underline{L}' = & \underline{\beta}3 & + Q2\ (Q3 + \ldots) & (\alpha 6 + \ldots) \\ & T3\ (\underline{H} + \underline{Q}3 + P1) & + Q2\ (Q3 + \ldots) & (S\ I1\ I2\ L + \ldots) \end{array}$$

The term H Q3 $\underline{P}$1 allows the carry logic to operate at sign time of even word periods.

The term P1 T3 replaces the normal off term for L.

Word Periods 4 to 63 For the remaining 61 word periods of multiplication the multiplicand, or zero, is added to the shifted partial product during every even word period depending on the state of P6, the multiplier bit. The addition is carried over into the odd word, and the new multiplier bit set is into P6 at the end of the odd word period. If the multiplicand is negative, a 1 is added to the partial product in every bit position to the left of the most significant bit of the multiplicand when the multiplier bit is a 1.

To denote word times 4 through 63 as different from 2 and 3, F is set on and remains on until the end of multiplication.

$$F' = \underline{F}\ \underline{G}\ H\ P1\ T3 + \ldots$$

The equations pertinent for these word periods are as follows:

$$\begin{array}{llll} I1 = & \multicolumn{3}{l}{A^{*}\ H\ F\ \underline{G} + \ldots} \\ I2 = & \multicolumn{3}{l}{\underline{G}\ H\ \underline{P1}\ P6\ R + H\ Q3\ P1\ P5\ P6} \\ L' = & \beta 3 & (\alpha 5 + \ldots \qquad) & + \ldots \\ & (\underline{T}3 + H\ Q3\ \underline{P}1) & (\underline{S}\ I1\ I2\ \underline{L} + \ldots) & + \ldots \end{array}$$

$$\begin{array}{llll} \underline{L}' = & \underline{\beta}3 & + Q2\ (Q3 + \ldots) & (\alpha 8 + \ldots) \\ & T3\ (\underline{H} + \underline{Q}3 + P1) & + Q2\ (Q3 + \ldots) & (\underline{S}\ \underline{I}1\ \underline{I}2\ L + \ldots) \end{array}$$

$$Aw' = (H\ \underline{T}3 + H\ \underline{P}1 + \ldots)\ (L\ I1\ I2 + L\ \underline{I}1\ \underline{I}2 + \underline{L}\ I1\ \underline{I}2 + \underline{L}\ \underline{I}1\ I2)$$

The flip-flop P1 continues to mark the even-odd word periods.

I1 copies A* during every word period. The first term of I2 is active for each even word-time; the second term, for each odd word period.

By the end of the 64th word period the full product is held in the two-word accumulator with the least significant bits having just been recorded. To retain the least significant bits of the product in the A register, the extended phase 4 is ended and phase 1 is entered, during which the normal A recirculation term continues to hold the least significant bits in A. In order to determine the last word period of multiplication, the sector address held in the track S1 is copied each word-time of phase 3 into the 4th through 10th bit positions of the C register as denoted by $\underline{S}2$ $\underline{S}3$.

$$Cw' = \underline{G}\ \underline{H}\ S1\ \underline{S}2\ \underline{S}3 + \ldots$$

When the correct address of the operand is found in phase 3, the last address copied into C is the address of the operand. When phase 4 is entered, this address is recirculated in C:

$$Cw' = G\ \underline{S2}\ C\ \underline{brc}\ (Q2 + \ldots) + \ldots$$

During the extended phase 4 the full contents of the C register is recirculated.

$$Cw' = H\ C\ \underline{brc} + \ldots$$

Since the end of multiplication exactly coincides with the word-time in which the operand address was located (because the $\underline{S2}$ $\underline{S3}$ portion of the S1 track is recorded so that addresses 64 word-times apart are identical), the address copied into the C register is used to seek agreement with the address appearing in the track S1. The flip-flop K is again used as the comparison device, being turned on at the beginning of each word period and set off when the digits of C and S1 disagree.

$$K' = T3\ \underline{Faf}\ (G + \ldots) + \ldots$$
$$\underline{K'} = H\ \underline{S1}\ \underline{S2}\ r1 + H\ S1\ \underline{S2}\ \underline{S3}\ r1 + \ldots$$
Where $r1 = C\ H + \ldots$

$\underline{S3}$ is included in the true comparison term, since S1 is true during sign digit time and would give a false comparison.

When K is found on at the end of sign time during word periods 4 through 63 as marked by F $\underline{G}$ H, F and H are set off and phase 1 is entered.

$$\underline{F'} = F\ H\ T3\ \underline{Q4}\ K + \ldots$$
$$\underline{H'} = H\ T3\ K\ \underline{Q4} + \ldots$$

It is necessary to include $\underline{Q4}$ to distinguish between Multiply M and Multiply N.

<u>Multiply M</u> ($\underline{Q1}$ Q2 Q3 Q4) Multiply A times V and retain the most significant digits of the product in A.

The process of Multiply M is carried out in a fashion identical to that for Multiply N, with the exception of the last word period. During this time the least significant digits are recorded in A, and the most significant digits are not available from A* until the next word time.

Phase 4 is not ended at this time but is extended an additional two word periods. During the 65th word period the most significant digits of the product are recorded in A. At the end of this word-time the product is one digit out of place (this is caused by multiplying by the spacer bit). One more word period, the 66th, is used to add A to A, effectively shifting the product one digit left. The 65th word-time is denoted by F G H P1. G is set on while F is left on.

$$G' = \underline{G}\ H\ T3\ K\ Ga\ Q4\ \underline{be} + \ldots$$
Where Q4 denotes Multiply M rather than N.

No changes are made in the P or the adder logic and the Aw' equation.

The next word period, denoted F G H $\underline{P1}$, is the last word period. The inputs to the adder are now A and A.

$$I1 = F\ G\ Q3\ \underline{P1}\ A + \ldots$$
$$I2 = G\ H\ Q3\ \underline{P1}\ A + \ldots$$
$$Aw' = (H\ \underline{P1} + \ldots)\ (L\ I1\ I2 + L\ \underline{I1}\ \underline{I2} + \underline{L}\ I1\ \underline{I2} + \underline{L}\ \underline{I1}\ I2)$$

At the end of word period 66, F, G, and H are set off and phase 1 is entered.

$\underline{F}' = F\ G\ T3\ \underline{P1} + \dots$
$\underline{G}' = G\ H\ T3\ Q3\ \underline{P1} + \dots$
$\underline{H}' = \beta 6 + \dots$
Where $\beta 6 = G\ H\ T3\ Q3\ \underline{P1}$

The word periods of the multiplication operations and the inputs and the outputs to the adder are simplified in Table 3-3 for reference.

TABLE 3-3 MULTIPLICATION $\underline{Q1}$ Q2 Q3

Word Period	F G H P1	Aw'	I1	I2	S	
1	1 1 0 X	A $\underline{T3}$	(A)	(V)		
2	0 0 1 0	Σ	0	P6R	1	
3	0 0 1 1	Σ $\underline{T3}$	A*	P5	1	
4	1 0 1 0	Σ	A*	P6 R	0	
5	1 0 1 1	Σ $\underline{T3}$	A*	P6 P5	0	
6, 8,... 62	1 0 1 0	Σ	A*	P6 R	0	
7, 9,... 63	1 0 1 1	Σ $\underline{T3}$	A*	P6 P5	0	
64	1 0 1 0	Σ	A*	P6 R	0	N ends here
65	1 1 1 1	Σ $\underline{T3}$	A*	P6 P5	0	
66	1 1 1 0	Σ	A	A	0	M ends here

Σ = Summation

Divide ($\underline{Q1}$ Q2 $\underline{Q3}$ Q4) Divide A by V and retain the rounded quotient in A.

The procedure for division is a non-restoring system in which each step brings the remainder toward zero by subtracting or adding the denominator as its sign agrees or disagrees with that of the remainder. It makes use of the extended accumulator to provide space for the storage of the growing set of quotient digits and to provide, by precession, for the doubling or shifting of the remainder at each step. As in multiplication, each step of division requires two word periods.

The denominator, V, is copied during the first word period of phase 4, into R; the sign being set into P5 as in multiply.

$Rw' = G\ \underline{H}\ V\ \underline{Q1}\ Q2\ \alpha 9 + \dots$
$P5' = G\ \underline{H}\ T3\ V\ P5a + \dots$
$\underline{P5}' = G\ \underline{H}\ T3\ \underline{V}\ P5a + \dots$
Where $\alpha 9 = Q3 + Q4$

During the first word-time of divide the sign of A is copied into P6 and held there for the next two word periods. At the same time the sign of the numerator in A is dropped from recirculation.

$P6' = F\ G\ \underline{H}\ T3\ A\ P6a + \dots$
$\underline{P6}' = F\ G\ \underline{H}\ T3\ \underline{A}\ P6a + \dots$
$Aw' = \underline{H}\ A\ \underline{To}\ [\underline{T3}\ \underline{Q1}\ Q2\ \alpha 9 + \dots] + \dots$
Where $\alpha 9 = Q3 + Q4$

Thereafter, the sign of each new remainder is set into P6 and held for two word periods. The new remainder is formed and recorded in each even word period. The sign of the remainder is then available at the A read head at sign time of the odd word periods.

$$P6' = H\ P1\ T3\ A\ \underline{Q3} + \ldots$$
$$\underline{P6'} = H\ P1\ T3\ \underline{A}\ \underline{Q3} + \ldots$$

During each pair of word periods of divide, the sign of the remainder is shifted one digit position, forming successive digits of the partial quotient. In each even word period from word-time 4 through 64, the doubled prior-remainder is corrected by the subtraction or addition of the denominator as the two signs held in P5 and P6 agree or differ. In the odd word periods, 3 through 65, the extended accumulator recirculates the partial quotient. Word periods 1; 2 and 3; 4 through 64; 65 and 66; and 67 are identified by $F\ G\ \underline{H}$, $\underline{F}\ \underline{G}\ H$, $F\ \underline{G}\ H$, $F\ G\ H$, and $\underline{F}\ G\ H$, respectively. For word period 2 the first digit of the quotient is formed:

$$I1 = \underline{F}\ \underline{G}\ \underline{Q3}\ \underline{P1}\ A + \underline{F}\ \underline{G}\ S1\ S3\ \underline{Q3}\ \underline{P1}\ P6 + \ldots$$

Where A = Numerator less sign

P6 = Sign of numerator

$$I2 = H\ \underline{Q3}\ \underline{P1}\ R + \ldots$$

$$L' = \begin{array}{l} \beta 3 \qquad (\alpha 5 + \alpha 7) + \ldots \\ (\underline{T3} + \ldots)\ (\underline{S}\ I1\ I2\ \underline{L} + S\ \underline{I1}\ I2\ \underline{L}) + \ldots \end{array}$$

$$\underline{L'} = \begin{array}{l} \beta 3 \qquad\qquad + Q2\ (\underline{Q1} + \ldots)\ (\alpha 6 + \alpha 8) \\ T3\ (\underline{Q3} + \ldots)\ + Q2\ (\underline{Q1} + \ldots)\ (S\ I1\ \underline{I2}\ L + \underline{S}\ \underline{I1}\ \underline{I2}\ L) \end{array}$$

$$Aw' = (H\ \underline{P1} + \ldots)\ (L\ \underline{I1}\ \underline{I2} + \underline{L}\ I1\ \underline{I2} + \underline{L}\ \underline{I1}\ I2 + L\ I1\ I2) + \ldots$$

$$S = H\ \underline{Q3}\ \underline{P5}\ \underline{P6} + H\ \underline{Q3}\ P5\ P6 + \ldots$$

For word period 3:

$$I1 = \underline{G}\ H\ \underline{Q3}\ P1\ A^* + \ldots$$
$$I2 = 0 \text{ (No copy term)}$$
$$Aw' - (H\ \underline{T3} + \ldots)\ (L\ \underline{I1}\ \underline{I2} + \underline{L}\ I1\ \underline{I2} + \underline{L}\ \underline{I1}\ I2 + L\ I1\ I2)$$

For the subsequent odd word-times:

$$I1 = H\ Q3\ P1\ A^* + \ldots$$
$$I2 = 0 \quad \text{(To prevent change of partial quotient, no term comes true.)}$$
$$Aw' = (H\ \underline{T3} + \ldots)\ (L\ \underline{I1}\ \underline{I2} + \underline{L}\ I1\ \underline{I2} + \underline{L}\ \underline{I1}\ I2 + L\ I1\ I2)$$

(Drop shifted MSD of numerator)

For the subsequent even word-times:

$$I1 = F\ \underline{G}\ H\ A^* + \ldots$$
$$I2 = H\ \underline{Q3}\ \underline{P1}\ R + \ldots$$

S, L, and A terms are as in word period 2.

By the end of 64 word periods the sector address coincidence occurs; however, the division process requires three more word periods to be completed. At sector coincidence, G is set on and remains on for two word periods.

$$G' = \underline{G}\ H\ T3\ K\ \underline{Ga}\ Q4\ \underline{be} + \ldots$$

At sign time of the second word period in which G is on, denoted by $\underline{P1}$, F is set off. G remains on, denoting the 67th word period.

$\underline{F'} = F\ G\ T3\ \underline{P1} + \ldots$

By the end of the 66th word period the full quotient is available in either its true or complemented form. Because of the system of division used, the factor determining whether the quotient is complemented or not is the sign of the denominator. If the sign of the denominator is positive, the quotient will always be complemented. The quotient is rounded by subtracting a 1 from each digit position if the sign of the remainder (the most significant digit of the remainder) and the sign of the denominator agree; otherwise, zeros are subtracted. Complementing and rounding occur simultaneously in the 67th word period.

$$I1 = \underline{F}\ G\ H\ \underline{A^*}\ \underline{P5} + G\ H\ \underline{Q3}\ P5\ A^* + \ldots$$
$$I2 = \underline{F}\ G\ H\ P5\ P6 + \underline{F}\ G\ H\ \underline{P5}\ \underline{P6} + \ldots$$
$$S = \underline{F}\ G\ H + \ldots$$
$$Aw' = (\underline{F}\ G\ H + \ldots)\ (L\ \underline{I1}\ \underline{I2} + \underline{L}\ I1\ \underline{I2} + \underline{L}\ \underline{I1}\ I2 + L\ I1\ I2)$$

At the end of the 67th word period division is ended, and phase 1 is entered by setting G and H off. The rounded quotient recirculates in A.

$$\underline{G'} = G\ T3\ \underline{F} + \ldots$$
$$\underline{H'} = \underline{F}\ G\ H\ T3 + \ldots$$

The simplified word periods for division are given in Table 3-4.

TABLE 3-4 DIVIDE $\underline{Q1}$ Q2 $\underline{Q3}$ Q4

Word Period	F G H P1	A'	I1	I2	S
1	1 1 0 X	A $\underline{T3}$	(A)	(V)	(1)
2	0 0 1 0	Σ	(A + T3 P6)	R	(P5 P6 + $\underline{P5}$ $\underline{P6}$)
3	0 0 1 1	Σ $\underline{T3}$	A*	0	(P5 P6 + $\underline{P5}$ $\underline{P6}$)
4	1 0 1 0	Σ	A*	R	(P5 P6 + $\underline{P5}$ $\underline{P6}$)
5-63	1 0 1 1	Σ $\underline{T3}$	A*	0	(P5 P6 + $\underline{P5}$ $\underline{P6}$)
6-64	1 0 1 0	Σ	A*	R	(P5 P6 + $\underline{P5}$ $\underline{P6}$)
65	1 1 1 1	Σ $\underline{T3}$	A*	0	(P5 P6 + $\underline{P5}$ $\underline{P6}$)
66	1 1 1 0	Σ	A*	R	(P5 P6 + $\underline{P5}$ $\underline{P6}$)
67	0 1 1 1	Σ	(P5 A* + $\underline{P5}$ $\underline{A^*}$) (P5 P6 + $\underline{P5}$ $\underline{P6}$)		1

Σ = Summation

3.7 INPUT-OUTPUT CIRCUITS

The following circuits are used in conjunction with input-output equipment. These circuits are physically located on the I/O cards. Since the input-output signals differ in nature from the computer signals, they are covered separately.

3.7.1 One-Shot Multivibrator

The primary purpose of the one-shot multivibrator, Figure 3-19, is to supply drive pulses to the electromechanical input/output devices. These input/output devices must have an applied signal which is long in duration, compared to the time of the signals used in the computer. For instance, the Tally Reader must have a 4.5 millisecond pulse applied to the escapement coil. The capacitor C1 is used to control the time of the on state of the one-shot; therefore, C1 is individually selected depending on the function performed.

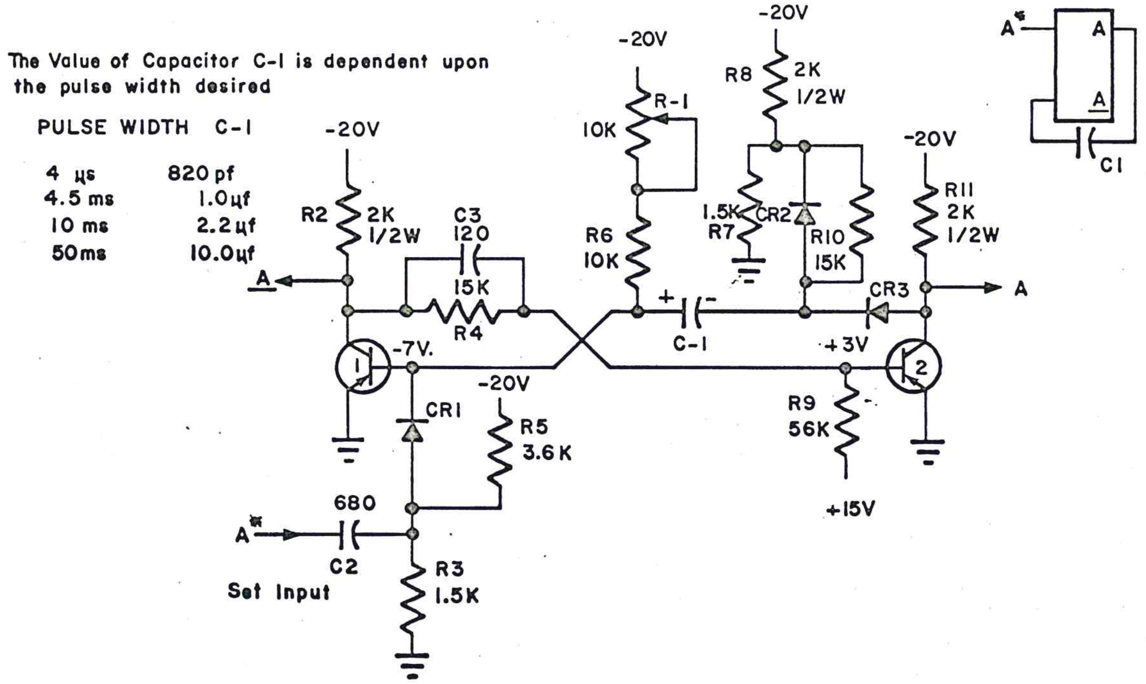


FIGURE 3-19 ONE-SHOT MULTIVIBRATOR

The one-shot exists in a stable state where A is the true output signal, and A is the false output signal. When an input signal is applied, the A* term going from false to true, the one-shot will change state and remain changed for a specified period of time.

With the input A* at a false level, Q1 is held in a conducting state and Q2 is cut off. Q1 is conducting by virtue of approximately -7V on its base, which is developed from the divider composed of R1, R6, CR1, R5, to -20V, and R3 to ground. Q2's base voltage is a function of the state of Q1 and is +3V, if Q1 is conducting, or -12V, if Q1 is cut off. These voltages are developed from the divider composed of either Q1 or R2, R4, and R9. C1 has -7V on the Q1 side and -8.5V on the Q2 side, or a net charge of 1.5V. The -8.5V is developed from the -20 supply, through R8 and R7 to ground.

When the input A* goes true, C2 and R3 differentiate the rise into a positive going 20V spike, from -7V to +13V, which is coupled through CR1 to the base of Q1 causing it to cut off. At the same instant that the 3V is applied to the base of Q1, C1 is able to charge to nearly 13V through the low impedance path composed of R8, CR2, and C1. C1 now has -8.5 volts on the Q2 side and +13 volts on the Q1 side, or a net charge of approximately 21 volts. When Q1 cut off, its collector dropped to approximately -18V. This caused the base of Q2 to drop from +3V to approximately -12V, so Q2 now begins to conduct. When Q2 conducts, it completes the discharge path for C1, which commences to discharge through CR3, Q2, to ground, through the power supply to R1, R6 to the more positive side of C1. The positive side of C1 is common with the base of Q1, so that as C1 bleeds off, its positive side falls off toward its static state of -7V at a rate contingent on the values of C1 itself, and potentiometer R1. When it has discharged to the point that Q1's base is no longer positive, Q1 begins to conduct. This returns ground to Q1's collector and +3V to Q2's base, cutting it off, and restoring the one-shot to its static state. It has thus completed one full cycle of output for one input and will now remain in this static condition until another input occurs. The one-shot will trigger only on the leading edge of an input signal. When the input returns to a false level, the spike generated by the differentiation of the trailing edge is unable to pass CR1.

The one-shot has a recovery time of about 1/3 its own period. Potentiometer R1 on each of the one-shots is adjustable, so that the time constant can be adjusted during preventative maintenance and field service conditions as required.

3.7.2 Astable Multivibrator

The astable, or free running, multivibrator generates a continuous train of complementary pulses from both of its outputs. (See Figure 3-20.) The A output will go true and the $\underline{A}$ output will go false for a specified period of time determined by the value of C1 and the setting of potentiometer R1. The width between pulses, when A is false and $\underline{A}$ is true, is determined by C2 and the setting of potentiometer R2. Therefore, the adjustment of R1 determines the pulse width, and the adjustment of R2 determines the width between pulses.

The astable multivibrator is not self starting; it receives an input from -20d which causes it to start.

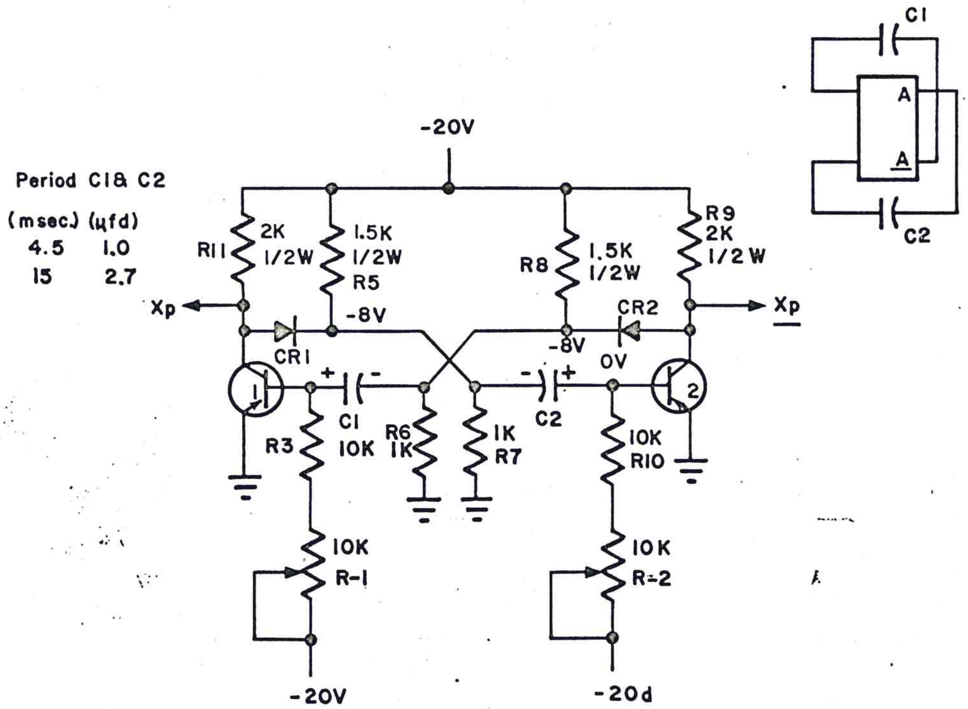


FIGURE 3-20 ASTABLE MULTIVIBRATOR

3.7.3 Storage Translator Driver

The storage translator driver, Figure 3-21, is essentially a bi-stable device whose output is capable of driving a large inductive load. Its characteristics are such that if both the A and B inputs are true Q1 will be cut off. With Q1 cut off, the base of Q2 will go negative, causing Q2 to conduct. When Q2 conducts, its collector goes positive, and the positive collector voltage is coupled back through CR1 to keep Q1 cut off. Therefore, this device will remain in this state regardless of what the state of the A and B inputs may be. The only way to reset the driver is to make input C negative. This causes Q1 to conduct and restores the driver to its off state. Q3 is a power transistor which conducts when Q2 is conducting, since its base is connected directly to the emitter of Q2. The output of Q3 is usually connected to a coil in an output device.

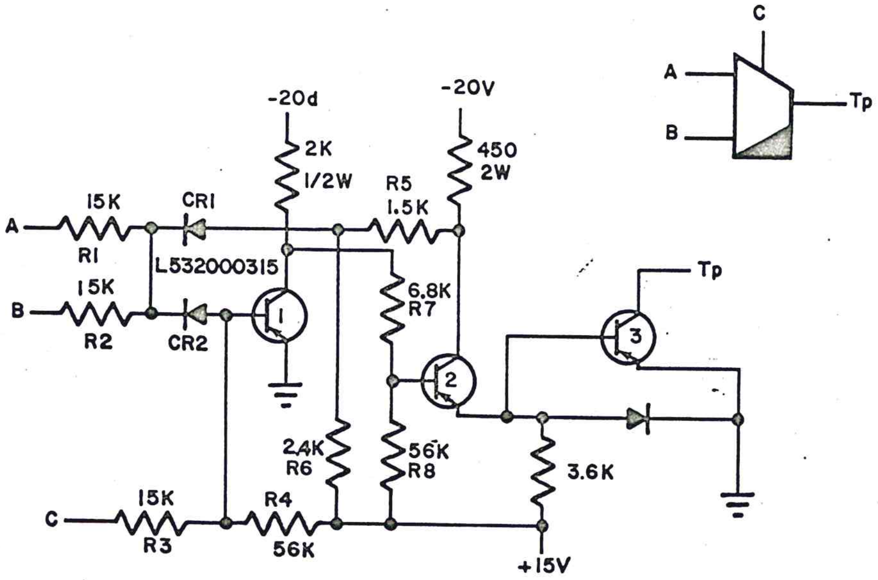


FIGURE 3-21 STORAGE TRANSLATOR DRIVER

In the quiescent, or off state, of the storage translator driver, Q1 is normally conducting, holding Q2 and Q3 cut off. Q1 is held in the conducting state by placing a negative potential on its base. This is accomplished by the voltage divider, consisting of R1 and R2.

In the non-energized state either input "A", input "B", or both are false (-20V). Therefore, either -10V or -20V is applied to the cathode of CR2. Since the plate of CR2 is returned to +15V through the 56K (R4), CR2 will be forward biased and Q1 will conduct. Also, since Q2 is cut off, there is a voltage divider from the -20V through R5 and R6 to the +15V supply, placing a negative voltage on the plate of CR1, back biasing CR1, and preventing circuit interaction.

During phase 1, sign time, of a print order both "A" and "B" inputs will come true applying zero volts to the voltage divider, consisting of R1 and R2. This voltage is applied to the base of Q1, cutting it off. The collector of Q1 then goes to -20 volts, forming a voltage divider consisting of R7 and R8 to the +15 volt supply, which places a negative potential on the base of Q2, causing it to conduct. The collector of Q2 goes to ground, and the voltage divider which consists of R5 and R6 places a positive potential on the anode of CR1, forward biasing it and coupling the positive potential through CR2 to hold Q1 cut off.

Since Q2 is an emitter follower, a negative signal on its base causes a negative swing on the emitter, which is directly coupled to the base of Q3. This causes Q3 to conduct, completing a path for current flow from a -48V source in the I/O equipment, through a channel magnet to ground, through Q3.

Q1 will remain cut off until the STC-3 CAM contacts close at 260° of the translator cycle in the Flexowriter, when placing -20V on the reset line "C". The voltage divider from this -20V through R3 and R4 to +15V places a negative potential on the base of Q1, back biasing CR2 and forcing Q1 into conduction. Q1's collector goes to zero volts which places a positive potential on the base of Q2, cutting it off. When Q2 cuts off, its collector goes to -20V which places a negative potential on the anode of CR1, back biasing it and allowing the inputs "A" and "B" to again become effective. At 300° of the translator cycle the reset line "C" is allowed to float, and Q1 is held in conduction by the circuit action described previously.

In the case of the Tally Punch, the reset pulse is the signal <u>Xp</u> and is at a -20V level for 13.5 ms beginning with the fall time of Rp.

3.7.4 Storage Clutch Driver

The storage clutch driver, Figure 3-22, is essentially the same as a storage translator driver, except that it requires only that the A input be true at clock time to set it on. This circuit will remain on until the B input goes negative. The output drives a clutch coil in an output device.

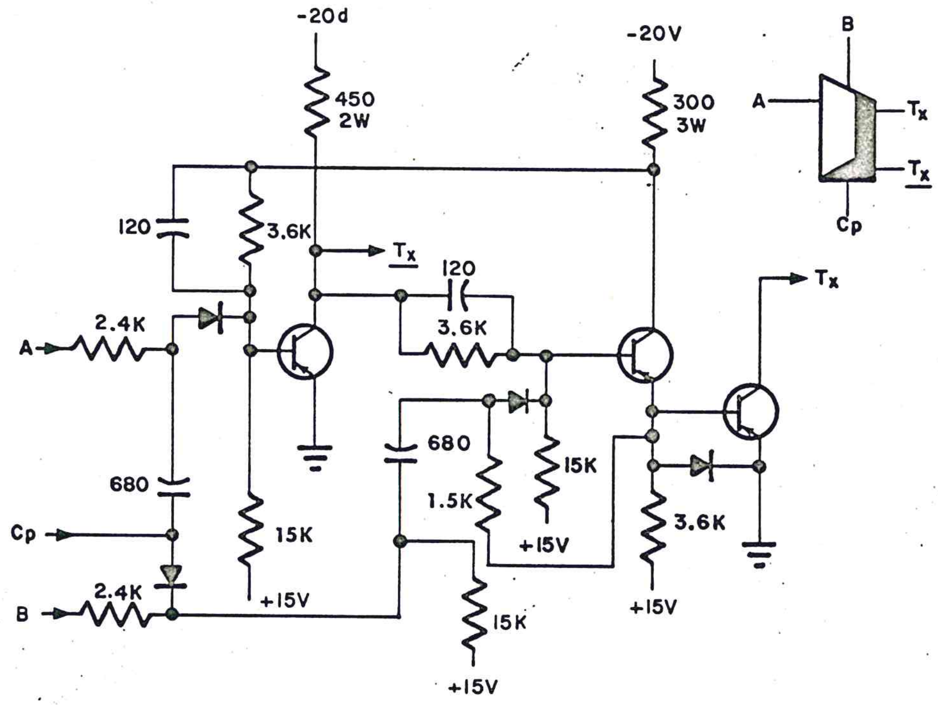


FIGURE 3-22 STORAGE CLUTCH DRIVER

3.7.5 Clutch Driver

The clutch driver, Figure 3-23, is essentially a power amplifier used to drive clutch coils on an input/output device. The output B will remain true only as long as input A is true.

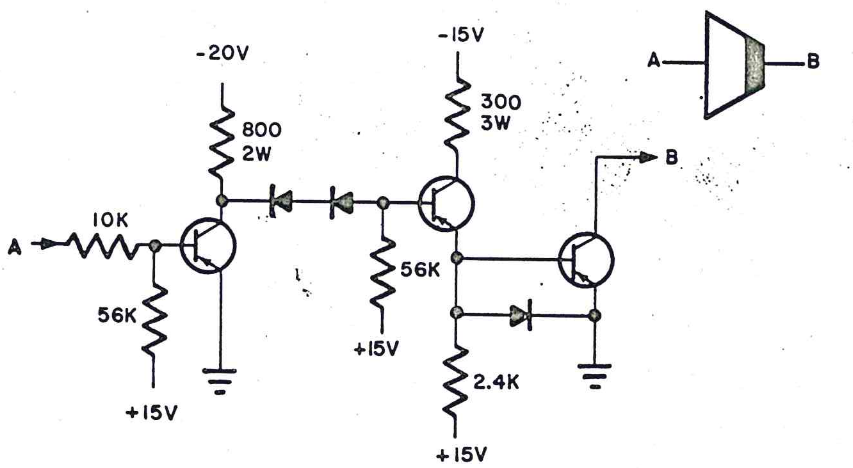


FIGURE 3-23 CLUTCH DRIVER

3.7.6 Translator Driver

The translator driver, Figure 3-24, is essentially a nor gate which drives a power amplifier. Both the A and B inputs must be true in order to have an output at C, which is connected to a coil in an input/output device. The C output will remain true only as long as both inputs remain true.

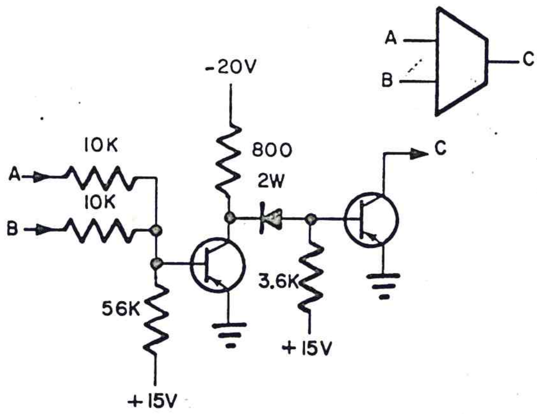


FIGURE 3-24 TRANSLATOR DRIVER

3.8 GENERAL I/O LOGIC

The logic of the LGP-21 is so arranged that most flip-flops have general control terms, which are distributed throughout the logic system (including the I/O boards) by means of the distribution board. This arrangement allows any I/O equipment (through its I/O board) to communicate with and thus control much of the LGP-21 logical operation. The applications of this will be seen when the I/O logic is studied in detail.

The Flex-Tally I/O Board has two flip-flops which are used for device selection. These are the Ff flip-flop which selects the Flexowriter and the Ft flip-flop which selects the Tally Reader. The Tally P and R I/O Board uses a common flip-flop Fy, which will select both the Tally Reader and the Tally Punch. The Fy signal is gated with Q3 to determine which device will be selected. Each of the I/O select flip-flops is turned on at sign time of phase 3 of an input or print instruction by addressing it with the track address of the instruction word. To illustrate, consider the Flexowriter flip-flop:

$$Ff' = F\ \underline{G}\ T3\ \underline{P1}\ \underline{P2}\ \underline{P3}\ \underline{P4}\ P5\ Q1\ \underline{Q2}\ \underline{Q3}\ \underline{Q4}\ \underline{be}\ \underline{Faf} + \ldots$$

$$F\ \underline{G}\ T3\ \underline{P1}\ \underline{P2}\ \underline{P3}\ \underline{P4}\ P5\ \underline{Q1}\ Q2\ \underline{Q3}\ \underline{Q4}\ \underline{be}\ \underline{Faf}$$

$\underline{Faf}$ is a general inhibit term which is off whenever any I/O flip-flop is on:

$$Faf = Ff + Ft + Fy + Fn + \ldots$$

Where n = I/O device designator

It is used through much of the main machine logic to set up specialized I/O conditions and, in each I/O flip-flop equation, to prevent more than one being on at one time.

The I/O instructions possess the option of operation in 4- or 6-bit mode, depending on whether the instruction is negative or positive, respectively. Since the sign bit of the instruction word is only available at sign time, the K flip-flop is used to store 4- or 6-bit mode information through the duration of the I/O instruction. This is possible since it is not needed for sector comparison during this period. K is set during sign time of phase 3:

$$K' = T3\ \underline{Faf}\ (R + \ldots) + bq$$

$$\underline{K}' = F\ \underline{G}\ T3\ \underline{R}\ Q1\ \underline{Q2}\ \underline{Q3}\ \underline{Q4}\ \underline{Faf} + F\ \underline{G}\ T3\ \underline{R}\ \underline{Q1}\ Q2\ \underline{Q3}\ \underline{Q4}\ \underline{Faf} + \ldots$$

bq is included in K' to force the 4-bit mode for manual input, and $\underline{\text{Faf}}$ is to prevent changing from 4-bit mode during manual input. $\underline{\text{Faf}}$ is also used in other $\underline{\text{K}}$' and K' terms to inhibit normal action of K during an I/O instruction. The K' term is further inhibited by T3 in an I/O instruction, since $\underline{\text{Faf}}$ does not go off soon enough:

$$K' = T3\ \underline{Faf}\ (\underline{F} + G + R + Q1 + \underline{Q2} + Q3 + Q4)\ (\underline{F} + G + R + \underline{Q1} + Q2 + Q3 + Q4) + \ldots$$

$\underline{\text{Print}}$ (Q1 $\underline{\text{Q2}}$ $\underline{\text{Q3}}$ $\underline{\text{Q4}}$) Print or punch the character represented by the most significant 4- or 6-bits (including the sign bit) in the accumulator on the output device specified by the track portion of the instruction address. The contents of the accumulator are unchanged. Phases 1 and 2 are normal. Phase 3 terminates in one word-time.

$$G' = F\ \underline{G}\ T3\ \underline{Q2}\ \underline{Q3}\ \underline{Q4}\ \underline{be}\ \underline{Faf} + \ldots$$

The I/O instruction possesses the option of operation in 4- or 6-bit mode, depending on whether the instruction is negative or positive, respectively. Since the sign bit of the instruction word is only available at sign time, the K flip-flop is used to store 4- or 6-bit mode information and retain this information through phase 4 and the following phase 1 as long as Faf remains true.

$$K' = T3\ \underline{Faf}\ (R + \ldots$$

K' is turned on if there is a 1 in the sign position of the R register, signifying a negative print instruction—thus 4-bit mode.

$$\underline{K}' = F\ \underline{G}\ T3\ \underline{R}\ Q1\ \underline{Q2}\ \underline{Q3}\ \underline{Q4}\ \underline{Faf}$$

$\underline{\text{K}}$' will turn K off if $\underline{\text{R}}$ is true at sign time indicating a positive print instruction—thus 6-bit mode. Simultaneously, the Ff flip-flop will be turned on at sign time of phase 3 to permit input or output operation and inhibit normal phase 1 operation.

$$Ff' = F\ \underline{G}\ T3\ Q1\ \underline{Q2}\ \underline{Q3}\ \underline{Q4}\ \underline{P1}\ \underline{P2}\ \underline{P3}\ \underline{P4}\ P5\ \underline{be}\ \underline{Faf}$$

P5 indicates a P 0200 (hexadecimal) instruction, and the Flexowriter will be used as the output device.

Phase 4 terminates in one word-time.

Set the P flip-flops into a shifting register from A. Recirculate A.

$$i = F\ G\ Faf$$
$$P1' = G\ i\ A$$
$$P2' = i\ P1$$
$$P3' = i\ P2$$
$$P4' = i\ P3$$
$$P5' = i\ P4$$
$$P6' = i\ P5$$

$$Aw' = \underline{H}\ A\ \underline{To}\ Q1\ \underline{Q3}\ \underline{Q4}$$

Also, at sign time of phase 4, Q3 must be set to indicate an output order.

$$Q3' = G\ T3\ Q1\ \underline{Q2}\ \underline{Q3}\ \underline{Q4}$$

Q2 will also be set at sign time of phase 4, so the computer will continue in normal operation after the print function begins to be executed.

$Q2' = F\ G\ T3\ \underline{Q1}\ \underline{Q2}\ (Q1 + Q3 + Q4 + P1 + P2 + P3 + P4 + P5 + P6)$

End phase 4.

$\underline{F}' = F\ G\ \underline{H}\ T3$
$\underline{G}' = G\ \underline{H}\ T3$

Begin the "PRINT" operation in phase 1, which is of a variable duration. At this time $\beta5$ inspects the state of the K flip-flop, which will determine 4- or 6-bit output.

$\beta5 = \underline{F}\ \underline{G}\ K\ Q3\ Faf$

If K is on, indicating 4-bit output, $\beta5$ is turned on. If $\beta5$ is on, P5 must be forced on and P6 off.

$P5' = \beta5$
$\underline{P6}' = \beta5$

X' will now determine the execution and the termination of the actual print function.

$X' = \underline{F}\ \underline{G}\ \underline{Tx}\ Q3\ T3\ Ff\ (JL\text{-}33)\ (KRC\ 23\text{-}24)\ (KFB\ 5\text{-}6)\ (STC\text{-}4)\ (KOC\ 3\text{-}4)$
Where Tx is the Flexowriter clutch driver signal to J17.

X will come true in phase 1 if $\underline{Tx}$ Q3 Ff and the following Flexowriter terms are in agreement for one bit time, i. e. T3.

$TP1 = XP1 \ldots\ldots TP6 = XP6$
$Tx = X$

If X' was allowed to come true, the print function is executed. As soon as X' came true, the print order is terminated, allowing the computer to search for the next instruction.

$\underline{Ff} = X$

$\underline{Ff}$ now makes $\underline{Faf}$ true. K' is now allowed to be turned on each sign time, and $\underline{K}'$ is allowed to turn K off if sector coincidence is not found. A normal phase 1 is being initiated.

When printing successive characters with print orders at maximum optimization, the computer will stop in blocked state phase 1 because X' cannot come true until $\underline{Tx}$ comes true (260 degrees of the translator cycle, controlled by the resetting of Tx by STC-3 cam in the Flexowriter) and J1-33 comes true at 310 degrees of the translator cycle controlled by STC-4 cam. If a preceding print order called for a Carriage Return, Tab, or Back Space, the computer will stop in blocked state phase 1 of the second print instruction because X' cannot come true until KFB 5-6 comes true, which will be after the Carriage Return, Tab, or Back Space has been completed.

Input ($\underline{Q1}\ Q2\ \underline{Q3}\ \underline{Q4}$) Enter information from an input device into the A register in 4- or 6-bit mode. The input device is selected by the track address of the instruction word. During input operations characters are read until either the input device puts out a stop signal or the input buffer senses a stop code. Characters enter the low order end of the A register and are shifted towards the high order end until a stop is received. As in the output command, phase 3 is terminated immediately.

$G' = F\ \underline{G}\ T3\ \underline{Q1}\ Q2\ \underline{Q3}\ \underline{Q4}\ \underline{be}\ \underline{Faf} + \ldots$

The K flip-flop will be used as an indicator of 4- or 6-bit mode.

$K' = T3\ \underline{Faf}\ (R + \ldots$
$\underline{K}' = F\ \underline{G}\ T3\ \underline{R}\ \underline{Q1}\ Q2\ \underline{Q3}\ \underline{Q4}\ \underline{Faf} + \ldots$

K on, gated by a negative input order, indicates 4-bit mode. K off, gated by a positive input order, indicates 6-bit mode.

The P flip-flops are gated to reset with the same T3 pulse that sets phase 4.

$$\mathrm{P1d} = \mathrm{P2d} = \mathrm{P3d} = \mathrm{P4d} = \mathrm{P5d} = \mathrm{P6d} = \mathrm{F}\ \underline{\mathrm{G}}\ \mathrm{T3}\ \underline{\mathrm{Q1}}\ \mathrm{Q2}\ \underline{\mathrm{Q3}}\ \underline{\mathrm{Q4}}\ \underline{\mathrm{be}}\ \underline{\mathrm{Faf}}$$
$$\mathrm{G'} = \mathrm{F}\ \underline{\mathrm{G}}\ \mathrm{T3}\ \underline{\mathrm{Q1}}\ \mathrm{Q2}\ \underline{\mathrm{Q3}}\ \underline{\mathrm{Q4}}\ \underline{\mathrm{be}}\ \underline{\mathrm{Faf}}$$
$$\mathrm{Ff'} = \mathrm{F}\ \underline{\mathrm{G}}\ \mathrm{T3}\ \underline{\mathrm{Q1}}\ \mathrm{Q2}\ \underline{\mathrm{Q3}}\ \underline{\mathrm{Q4}}\ \underline{\mathrm{P1}}\ \underline{\mathrm{P2}}\ \underline{\mathrm{P3}}\ \underline{\mathrm{P4}}\ \mathrm{P5}\ \underline{\mathrm{Faf}}\ \underline{\mathrm{be}}$$

Upon entering the dummy phase 4, the P flip-flop outputs are shifted into the A register:

$$\mathrm{i} = \mathrm{ic} = \mathrm{F}\ \mathrm{G}\ (\mathrm{Faf} + \underline{\mathrm{Q1}}\ \mathrm{Q2}\ \underline{\mathrm{Q3}}\ \underline{\mathrm{Q4}})$$
$$\mathrm{Aw'} = \mathrm{Ac1} = \mathrm{F}\ \mathrm{G}\ \underline{\mathrm{Q1}}\ (\mathrm{Faf} + \underline{\mathrm{Q1}}\ \mathrm{Q2}\ \underline{\mathrm{Q3}}\ \underline{\mathrm{Q4}})\ (\mathrm{K}\ \mathrm{P4} + \underline{\mathrm{K}}\ \mathrm{P6})$$

Where $\underline{\mathrm{Q1}}$ Faf indicates the input instruction, and K P4 + $\underline{\mathrm{K}}$ P6 indicates whether 4- or 6-bit shifting will take place.

The Flexowriter "turn on" one-shot is triggered:

$$\mathrm{Sr^*} = \mathrm{F}\ \underline{\mathrm{Q1}}\ \mathrm{Ff}\ \mathrm{Xs}\ \underline{\mathrm{bq}}$$

Where Xs indicates not in input mode.

Phase 4 is one word-time long.

Phase 1 is entered, and the computer will wait in this phase for a character to be presented. The 50 ms signal from the Sr one-shot is felt on KCRI.

$$\underline{\mathrm{G'}} = \underline{\mathrm{H}}\ \mathrm{T3}$$
$$\underline{\mathrm{F'}} = \mathrm{F}\ \mathrm{G}\ \underline{\mathrm{H}}\ \mathrm{T3}$$

KCRI picks, and Sr' is felt on KRC through the contacts 3-4 of KCRI. Relay KRC picks and then holds through KPE 21-22, KRC 3-4, SR-1, Stop Read switch and Start Compute switch to +48V. Sr times out and drops KCRI. This furnishes a pick path for KOC through STC-2, TB3, KFB 25-26, KCRI 21-22, KRC 3-4, SR-1, Stop Read and Start Compute switches to +48V. KOC will hold through its contacts 1-2, KRC 3-4, SR-1, Stop Read and Start Compute switches to +48V. The tape reader clutch is energized through KMI 1-2, KRC 5-6, KOC 25-26, SF-1, SF-4, KDC 3-4, SDC 1-2, Start Read switch, LKL 1-2, SBS, SCRT 1-2 to +48V.

When a character is read from tape, the respective reader contacts close causing the translator code magnets and clutch to be energized. The seeker selected trips the desired letter cam which prints character. Through operation of the related selector slide, the SC contacts are operated. Through $\underline{\mathrm{Ff}}$ logic (JL32) KOC 27-29, KRC 25-26, a negative level will be felt on SC-7 and the operated SC contacts. This sets the P flip-flops to the corresponding code, through the Pxc and Pxd terms. The next T3 after SC-7 1-2 make, phase 2 is skipped and phase 3 is entered by the term Fc.

$$\mathrm{F'} = \mathrm{Fc} = \underline{(\mathrm{JL12})}\ \underline{\mathrm{Sc}}\ \underline{\mathrm{Sk}}\ \mathrm{T3}\ \ldots$$
$$\mathrm{Sc} = \mathrm{P1}\ \underline{\mathrm{P2}}\ \underline{\mathrm{P3}}\ \underline{\mathrm{P4}}\ \underline{\mathrm{P5}}\ \underline{\mathrm{P6}}$$
$$\mathrm{Sk} = \mathrm{K}\ \underline{\mathrm{P5}}\ \underline{\mathrm{P6}}$$

Phase 3 will continue until the SC (P*) contacts are restored. As SC 2-3 make, the term Gc will terminate phase 3 and a one word-time phase 4 will occur.

$$\mathrm{G'} = \mathrm{Gc} = \underline{(\mathrm{JL11})}\ \underline{\mathrm{G}}\ \mathrm{F}\ \mathrm{T3}\ \ldots$$

In phase 4 the P flip-flops will be shifted into the A register. (Same logic of previous phase 4.)

Phase 4 is one word-time, and phase 1 is again entered to wait for the next character from tape. Phases 1, 3, and 4 will repeat for each character until a stop code is read.

The stop code will break reader contact SR-1, which drops relays KOC, KRC, and reader clutch magnet, LR.

The signal Xs will come true through KOC 21-22 and KRC 21-22.

$$\underline{Ff}' = \underline{F}\ \underline{G}\ \underline{Q3}\ T3\ \underline{Sr}'\ Xs\ \underline{bq}$$

The Flexowriter I/O flip-flop is reset allowing the term $\underline{Faf}$ to come true. A normal sector search is made for the next instruction, terminating the input order.

During Manual Input mode the negative level to SC-7 is supplied from $\underline{bq}$ logic through JL10.

<u>Left Shift</u> ($\underline{Q1}$ Q2 $\underline{Q3}$ $\underline{Q4}$) Shift the contents of the A register 4- or 6-bits to the left (toward the high order end). Shift zeros into the low order bit positions. The bits shifted out of the A register are lost.

Advantage is taken of the basic mode of operation of the input command by calling for an input from a non-existent input device. The only modification required to the input logic is

$$i = ic$$
$$\text{Where } ic = F\ G\ (\underline{Q1}\ Q2\ \underline{Q3}\ \underline{Q4} + \ldots) + \ldots$$

$$Aw' = Acl$$
$$\text{Where } Acl = F\ G\ \underline{Q1}\ (\underline{Q1}\ Q2\ \underline{Q3}\ \underline{Q4} + \ldots)\ (K\ P4 + \underline{K}\ P6)$$

Since Faf never comes on, the input mode is not extended beyond the first phase 4.

<u>Breakpoint Switches</u> (Tb1, Tb2, Tb3, Tb4) Explained under Sense command section.

<u>Transfer Control Switch</u> (Tc) Explained under Test command section.

<u>Entry Switches</u>

FILL-CLEAR (brc) The fill operation refers to filling the R register from the A register and is achieved as follows:

$$Rw' = A\ brc + R\ \underline{brc}\ \left[\underline{G} + \ldots\right] + \ldots$$

The clear operation refers to clearing the C register and is accomplished as follows:

$$Cw' = F\ S2\ C\ \underline{brc}\ (Q1 + \ldots) + \underline{G}\ S2\ C\ \underline{brc} + G\ \underline{S2}\ C\ \underline{brc}\ (\underline{F} + \ldots) +$$
$$H\ C\ \underline{brc} + \underline{G}\ T3\ \underline{brc} + \ldots$$

EXECUTE (be) The execute operation causes the machine to jump from phase 1 to phase 3 and to execute the command previously placed in the R register. The machine is held in phase 3 until the execute signal is removed, to prevent cycling caused by contact bounce.

$$F' = be\ T3 + \ldots$$

$\underline{be}$ is included in each term for G', see Section 3.10.1. The I/O flip-flops are also inhibited by be.

MODE

Normal Position. No special terms or operation.

One Operation Position (01). Explained under section on blocked state operation.

Manual Input Position (bq). The one operation position and the manual input position are electrically interlocked so that the one operation signal comes on before and stays on during the Manual Input mode. This means that the machine is in the blocked state mode during Manual Input mode. The manual input signal turns on the flip-flop assigned to the manual input device and input proceeds as explained under the input section. Using the Flexowriter as an example:

$$\underline{Q1'} = \underline{Q3'} = \underline{Q4'} = bq + \ldots$$
$$Ff' = bq + \ldots$$
$$\underline{Ff} = \underline{F}\ \underline{G}\ T3\ \underline{Q3}\ Xs\ \underline{Sr'}\ \underline{bq} + \ldots$$

START (bs). Explained under section on blocked state operation. The start button also contains a light which operates complementary to the Stop light and is de-energized by $\underline{F}\ \underline{G}\ \underline{Q2}$.

$\underline{I/O}$ (To). The I/O button, when depressed, clears the accumulator and turns off any I/O flip-flop that is on:

$$Aw' = \underline{To}\ \underline{H}\ A \left[F + G + \ldots \right] + \ldots$$
$$\underline{Ff'} = To + \ldots$$

The I/O button also contains a light that is turned on by the term Faf and thus indicates the I/O mode.

3.9 GLOSSARY OF LOGICAL FUNCTIONS

Flip-Flops

F, G, H	Phase flip-flops used to indicate phases 1 through 4 of the computing cycle. When H is false($\underline{H}$), $\underline{F}\ \underline{G} = \emptyset 1$, $\underline{F}\ G = \emptyset 2$, $F\ \underline{G} = \emptyset 3$, and $F\ G = \emptyset 4$. H is true only during extended phases used in multiply and divide.
Q1 → Q4	Order flip-flops used to hold the command during execution. Q1, Q2, and Q3 are time shared and are used as a skip indicator, blocked state indicator, and output command indicator, respectively.
P1 → P6	Track address and I/O flip-flops used to hold the track address during phases 1 and 3, and the character code during an I/O command. P1, P5, and P6 are time shared. P1 is used to indicate even and odd word-times of the extended phases; P5, to store the sign of the operand from memory; and P6, to store the sign of the A register in phase 4 plus holding successive bits of the multiplier or quotient.
K	Flip-flop used as a decision element to indicate sector coincidence in phases 1 and 3, as a carry flip-flop in phase 2 during addition of 1 to the C register, as a carry flip-flop in phase 4 during the addition of 1 to the C register in an "R" command, as a decision element in multiply or divide to indicate completion, and as an indicator of 4- or 6-bit mode during an I/O or left shift command.
L	Flip-flop used as the carry unit in arithmetic operations and to force a zero record in the spacer bit on any record order.
Fn	(n = I/O device designator) Flip-flop used to hold a specific I/O device on for the duration of the I/O command.

Logical Terms

i	Gates the P flip-flops together as a shifting register to load a track address or a character code to an output device.

α11	Gates the Q flip-flops together as a shifting register to load the order code during order time of phase 3.
I1	Adder input formed from the output of the A register, or other terms.
I2	Adder input formed from the output of a main memory location or other terms.
β3	Arithmetic carry term.
α5, α6, α7, α8	Overflow terms.
S	Used to control adder inputs for proper operation during subtract, multiply, or divide.
W	Used to gate the record signal on, during phase 4 of write orders.
rl	Forms proper input to the P flip-flop shifting register.
Kc	Forms blocked state term controlling stop light.
Faf	Forms I/O term indicating I/O mode of operation.

Record Terms

Aw'	Record signal for the A register (accumulator).
Cw'	Record signal for the C register (instruction counter).
Rw'	Record signal for the R register (instruction register).
Vw'	Record signal for main memory.

Read Terms

A	Playback from the A register.
A*	Playback from the A* register.
C	Playback from the C register.
R	Playback from the R register.
V	Playback from main memory.
S1	Playback of successive sector address digits for each T3 time.
S2	True for sector-and-track address time.
S3	True for track, order, and T3 time.
T3	Sign term formed from the logical AND of S1 and S3 signals.

Switch Terms

be	Execute position of entry switch
bQ	Manual Input mode
brc	FILL-CLEAR position of entry switch
bs	START COMPUTE switch
O1	One Operation mode
Tb1, 2, 3, 4	Breakpoint Switches
Tc	Transfer Control switch
To	I/O reset switch
Nna, b, c, d	(Nn = flip-flop or logical term designator.) In the case where Nn is a flip-flop, Nna and Nnb will be inhibit terms for the ON side and OFF side, respectively. Nnc and Nnd will indicate the set and reset term, respectively.

I/O Terms

Cd	Code delete gate for Tally reader, causes the reader to skip an input cycle.
Di	Synchronizing flip-flop for Tally Reader, prevents reader from coming on initially during the on cycle of free running multivibrator.
Ff	Flexowriter flip-flop, set on by Flexowriter select code on I/O.
Ft	Tally input flip-flop, set on by Tally select code on input.
JL11	Timing signals for Flexowriter end-of-input cycle.
JL12	Timing signals for Flexowriter start-of-input cycle.
Sc	Stop code gate for Tally reader.
Sr	One-shot multivibrator which readies Flexowriter for input.
Sr*	Input term to Sr one-shot multivibrator.
X	Flexowriter output gate flip-flop, gates storage drivers to Flexowriter.
Xp	Free-running multivibrator used to time Tally reader cycle.
Xs	Timing signal from Flexowriter indicating end of Flexowriter input. (Relay KOC is off.)
$\beta 5$	Defines Print in phase 1, 4-bit mode.

I/O Terms (Tally P and R Board)

$\underline{\text{Gc}}$	Set term for G flip-flop, which is inverted on the phase control board, to change from phase 3 to phase 4.

$\underline{Fc}$	Set term for F flip-flop, which is inverted on the phase control board, to change from phase 1 to phase 3, skipping phase 2.
$\underline{Fd}$	Reset term for F flip-flop, which is inverted on phase control board, to return to phase 1 from phase 3 inhibiting entry into phase 4.
Fy	Tally flip-flop.
Dtl	Tally reader clutch driver, operates sprocket drive.
Trl	Tally reader pulse to operating straps of star wheel contacts.
Rp	One-shot pulse of 4.5 ms duration, which controls duration of clutch driver pulses.
$\underline{Np}$	One-shot pulse of 6.0 ms duration, which provides an overlapping signal to Rp, to allow time for the reader-clutch to recycle.
Sc	Stop code gate for the Tally reader.
Sk	Inhibits entry of control characters to Tally reader in 4-bit mode.
$\underline{Cd}$	Not code deletes.
$\underline{Xp}$	Special one-shot circuit with a pulse duration of 13.5 ms, used to gate Rp and reset Tpg.
Pp	Tally punch output gate signal, which gates the storage translator drivers to the punch magnets.
Tpg	Storage clutch driver pulse, which drives the Tally sprocket punch and forward feed clutch magnet.
Dt	Tally reader clutch driver signal.
Tr	Tally reader character read signal.
Tx	Flexowriter clutch driver signal to J17.
P1* → P6* P1* → P6*	Character information from Flexowriter.
Tp1 → Tp6	Outputs of translator storage drivers for selecting translator magnets in Flexowriter.
Rs1 → Rs6 $\underline{Rs1}$ → $\underline{Rs6}$	Tally reader (1) star wheel contact signals for hole and no hole contacts respectively (negative signal).
Ry1 → Ry6 $\underline{Ry1}$ → $\underline{Ry6}$	Tally reader (2) star wheel contact signals for hole and no hole contacts respectively (negative signal).
Tpa → Tpf	Tpa - drive for channel punch magnet 1 Tpb - drive for channel punch magnet 2 Tpc - drive for channel punch magnet 3 Tpd - drive for channel punch magnet 4 Tpe - drive for channel punch magnet 5 Tpf - drive for channel punch magnet 6

$\underline{P1c} \rightarrow \underline{P6c}$		Input character information to set side of P flip-flops.
$P1d \rightarrow P6d$		Input character information to reset side of P flip-flops.
$\underline{Xpg}$		Tape feed switch tally punch.

3.10 LOGIC EQUATIONS

The following logic equations are divided into four sections, corresponding to the logical signals made up on each of the four printed circuit boards. An explanation of each term, or group of terms, within the equations is given.

Correlation between the schematics, Section 6, and the logic equations will enable accurate identification of logic signals and components.

3.10.1 Phase Control Board

F'	=	$\underline{F}\ \underline{G}\ H$	T3	P1	+	$\underline{F}\ G\ \underline{H}$	T3	$\underline{Q1}$ +	
		Ø4A	Sign time	W/P 3		Ø2	Sign time	Skip indicator	
		End W/P 3, Ø4A				Go to Ø3 if skip indicator is off			
		be	T3	+	Fc				
		Execute switch	Sign time		From input device				
		Execute at Sign Time			Go to Ø3 if character presented				

$\underline{F'}$	=	$F\ G\ \underline{H}$	T3		+	F G	T3	$\underline{P1}$ +	
		Ø4	Sign time			Ø4A	Sign time	P1 off	
		End Ø4				W/P 66 D. M			
		F H	T3	$\underline{Q4}$	K	+	Fd		
		Ø4A	Sign time	N	Sector comparison		Sc + Cd		
		W/P 64 "N" Multiply					Stop code or code delete		

G'	=	$F\ \underline{G}$	T3	$\underline{Q1}\ Q2\ \underline{Q3}\ \underline{Q4}$	$\underline{be}$	$\underline{Faf}$ +	
		Ø3	Sign time	Input	Not execute	I/O interlock	
		Enter Ø4 at sign time Ø3 on input order					

F $\underline{G}$ $\underline{H}$	T3	K	Ga	+
Ø3	Sign time	Sector comparison	$\underline{Faf}$ + $\underline{B1}$	

Enter Ø4 at sign time Ø3 after sector comparison

$\underline{G}$ $\underline{H}$	T3	K	Ga	Q2	$\underline{be}$	$\underline{bs}$	+
Ø1,3	Sign time	Sector comparison	$\underline{Faf}$	Not blocked state	Not execute	Not start	

Enter Ø2 after sector comparison if not in blocked state

$\underline{G}$ H	T3	K	Ga	Q4	$\underline{be}$	+
Ø4A	Sign time	Sector comparison	$\underline{Faf}$	D, M	Not execute	

End W/P 64 on D, M command

F $\underline{G}$	T3	Q1 $\underline{Q2}$ Q3	$\underline{be}$	+
Ø3	Sign time	U,T	Not execute	

Enter Ø4 after 1 word time on U,T command

F $\underline{G}$	T3	$\underline{Q2}$ $\underline{Q3}$ $\underline{Q4}$	$\underline{be}$	$\underline{Faf}$	+	Gc
Ø3	Sign time	Z,P	Not execute	I/O interlock		End of input cycle

Enter Ø4 after 1 word time on Z, P command

End input cycle

$\underline{G'}$	=	G $\underline{H}$	T3	+	$\underline{F}$ G	T3	+	G H	T3	Q3	$\underline{P1}$
		Ø4	Sign time		Ø2 W/P 67	Sign time		Ø4A	Sign time	M	P1 off
		End Ø4 after 1 word time			End Ø2 after 1 word time End Divide			End W/P 66 on M command			

H'	=	F G $\underline{H}$	T3	$\underline{Q1}$ Q2	α 9
		Ø4	Sign time		Q3 + Q4

Enter Ø4A after 1 word time Ø4 on D, N, M command

$\underline{H}$'	=	$\underline{F}$ G H	T3	+	H	T3	K	$\underline{Q4}$	+	β6
		Ø4A	Sign time		Ø4A	Sign time	Sector comparison	N		G H T3 Q3 $\underline{P1}$
		End W/P 67 D command			End W/P 64 N command					End W/P 66 M command

β6	=	G H	T3	Q3	$\underline{P1}$
		Ø4A	Sign time	M	P1 off
		End W/P 66 M command			

Kc	=	$\underline{F}$ $\underline{G}$	$\underline{Q2}$
		Ø1	Q2 off
		Blocked state	

Rw'	=	$\underline{F}$ G $\underline{H}$	V	+	G $\underline{H}$	V	$\underline{Q1}$ Q2	α 9	+
		Ø2	Copy main memory		Ø4	Main memory		Q3 + Q4	
		Copy main memory during Ø2			Copy main memory during Ø4 of D,N,M				

A	brc	+	R	$\underline{brc}$
Accumulator	Fill clear		Recirculate	Fill clear not depressed
Copy accumulator if "Fill Clear" is depressed			Recirculate R during	

[$\underline{G}$	+	H	+	F	($\underline{Q1}$	+	$\underline{Q2}$	+ $\underline{Q3}$ $\underline{Q4}$)]
Ø1,3		Ø4A		Ø4	P,E,U,T, H,C,A,S		Z,B,Y,R	I

Ø 1, 3, 4A and Ø4 of all commands except D, N, M

Vw'	=	$\underline{L}$	($\underline{Q1}$ Q4	K $\underline{C}$	+	$\underline{Q1}$ Q4	$\underline{K}$ C	+
		Force-record spacer bit to zero	R command	Complement C		R command	Copy C	

Augment count held in C by one

Q1	A	+	$\underline{Q4}$ A)
H,C	Accumulator		Y Accumulator
Copy Accumulator for H,C commands			Copy Accumulator for Y command

W	=	F G $\underline{H}$	Q1 Q2 $\underline{Q3}$	+	F G	S2	$\underline{Q1}$ $\underline{Q2}$ Q3
		Ø4	H,C		Ø4	Address time	Y,R

Ø4 of H,C command   Address time Ø4 of Y,R command

rl	=	$\underline{F}$	C	+	H	C	+	F $\underline{H}$	R	
		Ø1	Copy C		Ø4A	Copy C		Ø3	Copy R	

Ø1, 4A = C   Ø3 = R

Faf	=	Ff	+	Ft	+	Fn	+ . . .
		Flex on		Tally on		Next device	

K'	=	bQ	+	T3	$\underline{\text{Faf}}$	($\underline{F}$	+	G	+	R	+	
		Manual input		Sign time	I/O interlock	Ø1,2		Ø4		Negative I,P command		

Turn K on every sign time Ø 1, 2, 4
and I & P Commands Ø 3

Q1 + $\underline{Q2}$ + Q3 + Q4)

Any command but input

($\underline{F}$	+	G	+	R	+	Q1 + Q2 + Q3 + Q4)
Ø1, 2		Ø4		Negative command		Any command but print

Acl	=	F G	$\underline{Q1}$	(Faf	+	$\underline{Q1}$ Q2 $\underline{Q3}$ $\underline{Q4}$)
		Ø4	Input instruction	I/O mode		Input, shift

During Ø4 form 4 or 6 bit shifting register

(K	P4	+	$\underline{K}$	P6)
Negative command	Copy P4		Positive command	Copy P6

icl	=	F G	(Faf	+	$\underline{Q1}$ Q2 $\underline{Q3}$ $\underline{Q4}$)
		Ø4	I/O mode		Input, shift

Ø4, I/O mode, input or shift

P1d = P2d = P3d = P4d = P5d = P6d =	F $\underline{G}$	T3	$\underline{Q1}$ Q2 $\underline{Q3}$ $\underline{Q4}$
	Ø3	Sign time	Input, shift

$\underline{be}$	$\underline{Faf}$
Not execute	I/O interlock

Reset "P" Flip-Flops sign time Ø3 of input, shift command

P1b = P5a = P6a = ia = Ga =	$\underline{Faf}$
	I/O interlock

I/O interlock

T3 = S1 S3

Sign Time

3.10.2 P & Q Register Board

i =	ia	$\underline{G}$ $\underline{H}$	S2 S3 + ic
	$\underline{Faf}$	Ø1,3	Track Ø4, I/O Mode or Shift

Form shifting register with P flip-flops

P1' =	$\underline{G}$	i	r1	+	G	i	A	+
	Ø1,3	Shifting register	Ø1 = C Ø3 = R		Ø4	Shifting register	Copy A	

Copy track Ø1,3 — Copy A, Ø4, I, P

H	$\underline{P1}$	T3	+	P1c
Ø4A	Odd W/P	Sign time		From input device

Sign time odd W/P
D, N, M commands

$\underline{P1'}$ =	$\underline{G}$	i	$\underline{r1}$	+	G	i	$\underline{A}$	+
	Ø1,3	Shifting register	Ø1 = $\underline{C}$ Ø3 = $\underline{R}$		Ø4	Shifting register	Copy $\underline{A}$	

Copy track Ø1,3 — Copy $\underline{A}$, Ø4, I, P

H P1 T3 + G P1 T3 P1b + P1d

		Ø4A	Even W/P	Sign time		Ø4	P1 on	Sign time	I/O inter-lock	From input device
		Sign time even W/P D, N, M, commands				W/P 1, Ø4, D, N, M				

P2'	=	i	P1	+	P2c	
		Shifting register	Copy P1		From input device	
$\underline{P}$2'	=	i	$\underline{P}$1	+	P2d	
		Shifting register	Copy P1		From input device	
P3'	=	i	P2	+	P3c	
		Shifting register	Copy P2		From input device	
$\underline{P}$3'	=	i	$\underline{P}$2	+	P3d	
		Shifting register	Copy P2		From input device	
P4'	=	i	P3	+	P4c	
		Shifting register	Copy P3		From input device	
$\underline{P}$4'	=	i	$\underline{P}$3	+	P4d	
		Shifting register	Copy P3		From input device	
P5'	=	i	P4	+	P5c	+
		Shifting register	Copy P4		From input device	

G $\underline{H}$	T3	V	P5a	+	β5
Ø4	Sign time	Main memory	I/O interlock		Turn P5 on, Ø1, 4-bit mode, output command.

$\underline{P5}'$	=	i	$\underline{P4}$	+	P5d		+
		Shifting register	Copy P4		From input device		

G $\underline{H}$	T3	$\underline{V}$	P5a
Ø4	Sign time	Main memory	I/O interlock

Sign of operand, Ø4 D, N, M

P6'	=	i	P5	+	P6c	+	F G $\underline{H}$	T3	A	P6a	+
		Shifting register	Copy P5		From input device		Ø4	Sign time	Acc.	I/O inter-lock	

Sign of accumulator, Ø4 D, N, M

H	T3	P1	$\underline{Q3}$	A	+
Ø4A	Sign time	Odd W/P	Divide	Sign of remainder	

Sign of remainder, Odd W/P divide

H	T3	P1	Q3	A*
Ø4A	Sign time	Odd W/P	N, M	Multiplier

Multiplier bit, odd W/P, N, M

$\underline{P6}'$	=	i	$\underline{P5}$	+	P6d	+	F G $\underline{H}$	T3	$\underline{A}$	P6a	+
		Shifting register	Copy P5		From input device		Ø4	Sign time	Acc.	I/O inter-lock	

Sign of accumulator, Ø4 D, N, M.

H	T3	P1	$\underline{A}$	$\underline{Q3}$	+
Ø4A	Sign time	Odd W/P	Sign of remainder	Divide	

Sign of remainder, odd W/P divide

H	T3	P1	Q3	$\underline{A^*}$	+	β5
Ø4A	Sign time	Odd W/P	N,M	Multiplier		

Multiplier bit, odd

Turn P6 off, Ø1, 4 bit mode, output command

Q1'	=	a 11	R	+	G $\underline{H}$	T3	$\underline{Q1}$ $\underline{Q2}$ $\underline{Q3}$ $\underline{Q4}$	(R	$\underline{C}$	+
		Ø3 order	Copy R		Ø4	Sign time	Sense	Negative sense	Overflow toggle off	

Ø4, Sense command, breakpoint coincidence or negative sense, overflow toggle off.

P1 $\underline{Tb1}$ + P2 $\underline{Tb2}$ + P3 $\underline{Tb3}$ + P4 $\underline{Tb4}$)	$\underline{Faf}$	$\underline{To}$
Breakpoint coincidence	I/O interlock	I/O not depressed

$\underline{Q1}$'	=	a 11	$\underline{R}$	+	bq	+	G $\underline{H}$	T3	Q1
		Ø3 order	Copy R		MANUAL INPUT		Ø2,4	Sign time	Q1 on

End Ø4; Ø2 following skip

Q2'	=	a 11	Q1	+	$\underline{F}$ $\underline{G}$ $\underline{H}$	bs	+	F G	T3	$\underline{O1}$	$\underline{Q2}$	(Q1 +
		Ø3 order	Copy Q1		Ø1	start signal		Ø4	Sign time	Not ONE OPERATION		

Exit BLOCKED STATE Ø4, not ONE OPERATION, not STOP

Q3 + Q4 + P1 + P2 + P3 + P4 + P5 + P6)

$\underline{Q2}$'	=	a 11	$\underline{Q1}$	+	$\underline{H}$'	O1	+	G	T3	Q1	O1 +
		Ø3 order	Copy Q1		End D, N,M	One operation		Ø4	Sign time	P,E,U, T,H,C, A,S	ONE OPERATION

Enter BLOCKED STATE

G	T3	$\underline{Q1}$ Q2 $\underline{Q3}$ $\underline{Q4}$	O1	+	To
Ø4	Sign time	Input	ONE OPERATION		I/O RESET

Ø4 input, ONE OPERATION

Q3'	=	a 11	Q2	+	G	T3	Q1 $\underline{Q2}$ $\underline{Q3}$ $\underline{Q4}$
		Ø3 order	Copy Q2		Ø4	Sign time	Print

Ø4 Sign time, print

$\underline{Q3}' = \alpha 11 \quad \underline{Q2} \quad + \quad bq$

Ø3 order	Copy Q2	MANUAL INPUT

$Q4' = \alpha 11 \quad Q3$

Ø3 order	Copy Q3

$\underline{Q4}' = \alpha 11 \quad \underline{Q3} \quad + \quad bq \quad + \quad T3 \quad Q1\ \underline{Q2}\ Q3 \cdot A \quad +$

Ø3 order	Copy Q3	MANUAL INPUT	Sign time	Test	Accumulator negative

$T3 \quad Q1\ \underline{Q2}\ Q3 \quad R \quad Tc$

Sign time	Test	Negative	TRANSFER CONTROL

Transfer on negative test, transfer control

$\alpha 9 = Q3 + Q4$

$\alpha 11 = F\ \underline{G}\ \underline{H}\ \ \underline{S1}\ \underline{S2}\ S3 \quad \underline{bq} \quad \underline{Faf}$

Ø3	Order time	Not MANUAL INPUT	I/O interlock

$\beta 5 = \underline{F} \quad \underline{G} \quad K \quad Q3 \quad Faf$

Ø1	4-Bit mode	Output indicator	I/O mode

Ø1 Print, 4-bit mode

3.10.3 Arithmetic Board

$Aw' = F\ G\ \underline{H}\ \ \underline{Q2}\ \underline{Q3}\ Q4 \quad V \quad (\underline{Q1} \ + \ A) \quad +$

Ø4	B,E Command	Copy main memory	B	AND with accumulator

Ø4 copy main memory on B, AND with A on E.

$\underline{H} \quad A \quad \underline{To} \quad [\underline{F} \ + \ \underline{G} \ +$

Not Ø4A	Recircu-late	I/O switch not operated	Ø1, 2 Ø3

Recirculate Ø 1, 2, 3, Ø4 P, H, U, T, Y, R, Z and all but sign bit Ø4 D, N, M

$Q1\ \underline{Q3}\ \underline{Q4}$	+	$\underline{T3}$	$\underline{Q1}\ Q2$	$\alpha 9$	+
P, H		Not sign time	D,N,M	(Q3 + Q4)	

$\underline{Q2}$	$(Q3 + \underline{Q4})$	$\underline{Faf}$	+	Acl	+
U, T, Y, R, Z		Not I/O		Shifting register	

$$[\beta 1\ (L\ \underline{I1}\ \underline{I2} + \underline{L}\ I1\ \underline{I2} + \underline{L}\ \underline{I1}\ I2 + L\ I1\ I2)]$$

Copy adder logic

$\beta 1$ =	$H\ \underline{T3}$	+	$H\ \underline{P1}$	+	$\underline{F}\ G\ H$	+ F G		Q1 Q2 Q3
	Ø4A, except sign time		Ø4A even W/P		W/P 67 Divide	Ø4		A,S

During Ø4A, except odd W/P sign time, W/P 67 D, and Ø4A, S command, copy adder logic.

Cw' =	F	S2	C	$\underline{brc}$	$(\underline{Q1} + Q2 + \underline{Q3} + Q4)$ +
	Ø3,4	Address time	Recirculate	Not FILL-CLEAR	Not U command

Recirculate address Ø4, not U command

$\underline{G}$	S2	C	$\underline{brc}$	+	H	C	$\underline{brc}$	+
Ø1,3	Address time	Recirculate	Not FILL CLEAR		Ø4A	Recirculate	Not FILL CLEAR	

Recirculate address Ø1,3

G	$\underline{S2}$	C	$\underline{brc}$	$(\underline{F}$ +	$\underline{T3}$	+	$\underline{R}$	+
Ø2,4	Not address time	Recirculate	Not FILL CLEAR	Ø2	Not sign time		Not negative command	

Recirculate all but address except sign time Ø2 negative Z order.

Q1 + Q2 + Q3 + Q4	+	Faf	+	To	)	+
Any command but Z		I/O mode		I/O RESET		

$\underline{F}\ G\ \underline{H}$	S2	$C\ \underline{K}$	+	$\underline{F}\ G\ \underline{H}$	S2	$\underline{C}\ K$	+
Ø2	Address time	Copy C		Ø2	Address time	Complement C	

Augment C register during Ø2

$\underline{G}$	T3	C	$\underline{brc}$ +	G $\underline{H}$	S1 $\underline{S2}$ $\underline{S3}$ +
Ø1,3	Sign time	Recircu- late	Not FILL CLEAR	Ø1,3	High order sector iden- tification

Recirculate sign bit Ø1,3 — Copy high order sector Ø1,3

F G	T3	Q1 Q2 Q3	(α 5 + α 6 + α 7 + α 8
Ø4	Sign time	A, S command	($\underline{S}$ I1 I2 $\underline{L}$ + S I1 $\underline{I2}$ L + S $\underline{I1}$ I2 $\underline{L}$ + $\underline{S}$ $\underline{I1}$ $\underline{I2}$ L) Adder Logic

Set overflow toggle, sign time Ø4, A, S command

F G $\underline{H}$	$\underline{T3}$	Q1 $\underline{Q2}$ Q3 $\underline{Q4}$	R +
Ø4	Not sign time	U command	Copy R

Copy R Ø4 U command except sign time.

$\underline{F}$ $\underline{G}$ H	T3	$\underline{Q3}$	P1 P6 A +
W/P2	Sign time	Divide	Indicates overflow
$\underline{F}$ $\underline{G}$ H	T3	$\underline{Q3}$	P1 $\underline{P6}$ $\underline{A}$
W/P2	Sign time	Divide	Indicates overflow

Set overflow toggle W/P2 Divide

I1 =	$\underline{F}$ G H	$\underline{A^*}$	$\underline{P5}$ +	G H	$\underline{Q3}$	P5	A* +
	W/P67 Divide	Copy $\underline{A^*}$	Negative denominator	W/P 65, 66, 67	Divide	Posi- tive Denomi- nator	Copy A*

Complement quotient — Copy quotient, W/P 65, 66, 67

F G $\underline{P1}$	Q3	A +	$\underline{F}$ $\underline{G}$ $\underline{P1}$ $\underline{Q3}$	A +
W/P 66	M multiply	Copy accumu- lator	W/P 2 Divide	Copy accumulator

W/P 66, M, Copy accumulator W/P2, D, copy accumulator

$\underline{F}$ $\underline{G}$ $\underline{P1}$	S1 S3	$\underline{Q3}$	P6	+ F $\underline{G}$ H	A* +
W/P 3	Sign time	Divide	Copy sign of numerator	W/P 4-64	Copy A*

W/P 3 sign time, D, copy sign of numerator W/P 4-64, Copy A*

H P1	Q3	A*	+	F H	$\underline{Q3}$	A*	+	$\underline{G}$ H P1	$\underline{Q3}$	A*	+
Odd W/P 3-65	N,M	Copy A*		W/P 65,66	D	Copy A*		W/P 3	D	Copy A*	

Odd W/P 3-65 N,M copy A* | W/P 65, 66, D, Copy A* | W/P3, D, Copy A*

$\underline{H}$	A
Not Ø4A	Copy A

I2	=	$\underline{F}$ G H	P5 P6	+	$\underline{F}$ G H	$\underline{P5}$ $\underline{P6}$	+	H $\underline{P1}$	$\underline{Q3}$	R	+
		W/P 67			W/P 67			Even W/P 4-64	Divide	Copy R	

Round-off quotient | Copy R even W/P 4-64, Divide

$\underline{G}$ H $\underline{P1}$	P6	R	+	G H $\underline{P1}$	Q3	A	+
Even W/P 2-64	Multi-plier digit	Copy R		W/P 66	M	Copy A	

Copy R even W/P 2-64 if multiplier digit is one | Copy A during W/P 66 M command

$\underline{F}$ H P1	Q3	P5	+	H P1	Q3	P5 P6	+	$\underline{H}$ V
W/P 3	N,M	Copy sign of multipli-cand		Odd W/P 5-65	N,M	Multiplier, multipli-cand sign		Copy main memory except Ø4A

Copy sign of multipli-cand W/P 3, M, N command | Copy ones odd W/P 5-65, N, M if multiplicand sign and multiplier are ones.

$\underline{K'}$	=	G $\underline{H}$	S2	$\underline{C}$	$\underline{Faf}$	($\underline{F}$	+	Q3)	+
		Ø2,4	Address time	First zero	Not I/O mode	Ø2		Ø4, R command	

Indicate first zero in C for complementing

H	$\underline{S1}$ $\underline{S2}$	r1	+	H	S1 $\underline{S2}$ $\underline{S3}$	$\underline{r1}$	+
Ø4A	High order sector	r1 = C		Ø4A	High order sector	$\underline{r1}$ = $\underline{C}$	

Indicate no sector coincidence, Ø4A

$\underline{G}\ \underline{H}$	$\underline{S1}\ S2\ \underline{S3}$	rl	$\underline{Faf}$ +	$\underline{G}\ \underline{H}$	$S1\ S2\ \underline{S3}$	$\underline{rl}$	$\underline{Faf}$ +
Ø1,3	Sector identification	rl=C (Ø1) rl=R (Ø3)	Not I/O mode	Ø1, 3	Sector identification	rl=C $\overline{(Ø1)}$ rl=R $\overline{(Ø3)}$	Not I/O mode

Indicate no sector coincidence, Ø1, 3

F $\underline{G}$	T3	$\underline{R}\ Q1\ \underline{Q2}\ \underline{Q3}\ \underline{Q4}$	$\underline{Faf}$ +
Ø3	Sign time	Positive Print command	Not I/O mode

End Ø3 in 1 word-time on
positive print command

F $\underline{G}$	T3	$\underline{R}\ \underline{Q1}\ Q2\ \underline{Q3}\ \underline{Q4}$	$\underline{Faf}$
Ø3	Sign time	Positive input or shift command	Not I/O mode

End Ø3 in 1 word-time on positive
input or shift command

L' =	W +	F G	$\underline{Q2}$ +	B3
	Record	Ø4	Y,R	($\underline{T3}$ + H Q3 $\underline{P1}$)
	1-Bit delay for H, C	Permit recording first address bit Y,R commands		Any time except sign time, and even W/P N,M commands during sign time

(α 5 + α 7)'

($\underline{S}$ I1 I2 $\underline{L}$ + S $\underline{I1}$ I2 $\underline{L}$)

Copy carry logic

$\underline{L}$' =	$\underline{β}$3 +	Q2 ($\underline{Q1}$ + Q3)	(α 6 + α 8)
	T3 ($\underline{H}$ + $\underline{Q3}$ + P1)	D, N, M, A, S	(S I1 $\underline{I2}$ L + $\underline{S}$ $\underline{I1}$ $\underline{I2}$ L)
	Sign time of all normal phases, divide, odd W/P N, M commands	D, N, M, A, S commands, copy carry logic	

S =	$\underline{H}$ Q4 +	H $\underline{Q3}$	$\underline{P5}$ $\underline{P6}$ +	H $\underline{Q3}$ P5 P6 +
	Subtract	Divide		Divide

Divide, denominator and numerator
signs are alike.

$\underline{F}$ H Q3	+	$\underline{F}$ G H
W/P 2,3 N, M commands		W/P 67 divide

$\alpha 5 = \underline{S}\ \ I1\ \ I2\ \ \underline{L}$

$\alpha 6 = S\ \ I1\ \ \underline{I2}\ \ L$

$\alpha 7 = S\ \ \underline{I1}\ \ I2\ \ \underline{L}$

$\alpha 8 = \underline{S}\ \ \underline{I1}\ \ \underline{I2}\ \ L$

$\beta 3 = \underline{T3} + H\ Q3\ \underline{P1}$

3.10.4 Flex-Tally I/O Board

Fc	=	($\underline{JL}$ 12)	T3	$\underline{Sc}$	$\underline{Sk}$	+
		Start input cycle	Sign time	Not Stop Code	Not Control Character	

Enter Ø3, Not Stop Code, Not Control Character

$\underline{F}$ $\underline{G}$	T3	Rp	$\underline{Sc}$	$\underline{Cd}$	Ft	$\underline{Sk}$
Ø1	Sign time	Tally inputting	Not stop code	Not code delete	Tally input	Not Control Character

Tally reader presenting character

Fd	=	F $\underline{G}$	T3	(Sc + Cd + Sk)	(Ff + Ft) ·
		Ø3	Sign time	Stop code, Code delete, or Control Character	Flex or Tally input

Reading stop code or code delete from input device

Gc	=	($\underline{JL}$ 11)	F $\underline{G}$	T3	+	F $\underline{G}$	T3	$\underline{Rp}$	Ft
		End of Flex input cycle	Ø3	Sign time		Ø3	Sign time	End of Tally input	Tally reader on

Enter Ø4 at end of character

Enter Ø4 at end of character from Tally.

Ff'	=	F $\underline{G}$	T3	$\underline{P1}$ $\underline{P2}$ $\underline{P3}$ $\underline{P4}$ P5	Q1 $\underline{Q2}$ $\underline{Q3}$ $\underline{Q4}$	$\underline{be}$	$\underline{Faf}$	+
		Ø3	Sign time	01, Flex select code	Print	Not EXECUTE	I/O interlock	

Select Flex for print command

bQ	+	F $\underline{G}$	T3	$\underline{P1}$ $\underline{P2}$ $\underline{P3}$ $\underline{P4}$ P5	$\underline{Q1}$ Q2 $\underline{Q3}$ $\underline{Q4}$	$\underline{be}$	$\underline{Faf}$
MANUAL INPUT		Ø3	Sign time	01, Flex select code	Input	Not EXECUTE	I/O inter- lock

Select Flex for input command

$\underline{Ff'}$ =	$\underline{F}$ $\underline{G}$	T3	$\underline{Q3}$	Xs	$\underline{Sr'}$	$\underline{bQ}$	+
	Ø1	Sign time	Output command indicator	End of input	Flex ready for input	Not in MANUAL INPUT	

Reset Flex at end of input

X	+	To
Print		I/O reset

Ft' =	F $\underline{G}$	T3	$\underline{P1}$ $\underline{P2}$ $\underline{P3}$ $\underline{P4}$ $\underline{P5}$	$\underline{Q1}$ Q2 $\underline{Q3}$ $\underline{Q4}$	$\underline{be}$	$\underline{Faf}$
	Ø3	Sign time	00, Tally select code	Input	Not EXECUTE	I/O interlock

Select Tally reader for input command

$\underline{Ft'}$ =	$\underline{F}$ $\underline{G}$	T3	Sc	$\underline{Xp}$	+	To
	Ø1	Sign time	Stop code	Tally reader multivibrator		I/O reset

Reset Tally reader on stop code

Rp =	Xp	Di
	Tally reader multivibrator	Tally reader sync.

Dt = Rp

Start Tally input

Sc = P1 $\underline{P2}$ $\underline{P3}$ $\underline{P4}$ $\underline{P5}$ $\underline{P6}$

Stop code

Cd = P1 P2 P3 P4 P5 P6

Code delete

Di' =	$\underline{F}$ $\underline{G}$	$\underline{Xp}$	Ft
	Ø1	Tally reader multivibrator	Tally input

$\underline{Di}$' =	$\underline{Faf}$
	I/O interlock

Sr* =	F	$\underline{Q1}$	Xs	$\underline{bQ}$	Ff
	Ø4	Input	Not in input mode	Not MANUAL INPUT	Flex Selected

X' =	$\underline{F}$ $\underline{G}$	T3	$\underline{Tx}$	(JL 33)	Q3	Ff
	Ø1	Sign time	Clutch driver not set	Translator cam	Output command indicator	Flex se-lect

Ø1 sign time output command to Flex

$\underline{X}$' =	F +	G +	$\underline{T3}$ +	Tx +	($\underline{JL}$ 33) +
	Ø3,4	Ø2	Any time except sign time	Translator clutch driver	Translator cam
	$\underline{Q3}$ +	$\underline{Ff}$			
	Output command indicator	Flex not selected			

Tp1 =	X	P1
	Print	P1 bit

Tp2 =	X	P2
	Print	P2 bit

Tp3 =	X	P3
	Print	P3 bit

Tp4 =	X	P4
	Print	P4 bit

Tp5 =	X		P5
	Print		P5 bit

Tp6 =	X		P6
	Print		P6 bit

Tx =	X	=	JL 7
	Print		Signal to translator clutch

Translator driver reset = (JL 29)

Signal from Flex

Sk =	$\underline{P5}$ $\underline{P6}$	K
	Control Character	4 bit

Inhibit entrance of Control Characters in 4 bit.

3.10.5 Tally P and R Board

Gc =	F $\underline{G}$	T3	Fy	$\underline{bs}$	$\underline{Rp}$
	Phase 3	Sign time	Tally select	Not MANUAL INPUT	Tally clutch signal

Enter Ø 4 at end of character from Tally

Fc =	$\underline{F}$ $\underline{G}$	T3	$\underline{Q3}$	Fy	Rp	$\underline{Sk}$
	Ø 1	Sign time	Output command indicator	Tally select	Tally clutch signal	Not Contol Character
	$\underline{Cd}$		$\underline{Tpg}$			
	Not Code Delete		Not driving Tally punch			

Enter Q3, from Ø 1, Tally reader presenting character

Fd =	F $\underline{G}$	T3	Fy	(Cd + Sc + Sk)	
	Ø 3	Sign time	Tally select	Code Delete, Stop Code, or Control Char.	

Enter Q1 after reading Code Delete, Stop Code, or Control Character from Tally Reader

Fy'	=	F $\underline{G}$	T3	$\underline{Q1}$ Q2 $\underline{Q3}$ $\underline{Q4}$	$\underline{P1}$ $\underline{P2}$ $\underline{P3}$ P4 P5
		Ø 3	Sign time	Input	Tally select code

Enter Ø 1, select Tally reader for input

$\underline{be}$	$\underline{Faf}$	+	F $\underline{G}$	T3	Q1 $\underline{Q2}$ $\underline{Q3}$ $\underline{Q4}$
Not EXECUTE	I/O Interlock		Ø 3	Sign time	Print

$\underline{P1}$ $\underline{P2}$ $\underline{P3}$ P4 P5	$\underline{be}$	$\underline{Faf}$	+	$\underline{Faf}$	bs	bQ
Tally select	Not EXECUTE	I/O Interlock		I/O Interlock	START COMPUTE	MANUAL INPUT

Enter Ø 1, select Tally punch for output. I/O Interlock

$\underline{Fy'}$	=	$\underline{F}$ $\underline{G}$	T3	$\underline{Q3}$	$\underline{bs}$	$\underline{Rp}$	Sc
		Ø 1	Sign time	Output command indicator	Not start signal	Tally clutch signal	Stop Code

Enter Ø 3 or Ø 4, reset Tally reader on Stop Code

+	To	+	Pp
	I/O Reset		Punch clutch selected

I/O reset switch, reset Tally after output cycle

$\underline{Trl}$	=	$\underline{Q3}$	Rp	Fy	$\underline{Tpg}$
		Output command indicator	Tally clutch signal	Tally select	Not driving Tally punch

Reset Tally flip-flop

Dtl	=	$\underline{Trl}$
		Reader forward

Np*	=	Rp
		Fire Np one-shot

Rp*	=	$\underline{Xpg}$	$\underline{Np}$ $\underline{Xp}$	+	$\underline{Xp}$ $\underline{Np}$	Fy	$\underline{G}$	T3
		Tape Feed Switch	Not output Tally		Not output Tally	Tally select	Ø 1 or Ø 3	Sign time

Fire Rp one-shot

$\underline{Rp}$	=	Xp

Reset Rp flip-flop

Tpg	=	$\underline{Xpg}$	Rp	+	Q3	Fy	Rp	$\underline{Tpg}$
		Tape Feed Switch	Tally clutch signal		Output command indicator	Tally select	Tally clutch signal	Not driving Tally clutch

$\underline{Tpg}$	=	$\underline{Xp}$

Pp	=	Q3	Fy	Rp	$\underline{Tpg}$
		Output command indicator	Tally select	Tally clutch signal	Not driving Tally clutch

Sc = P1 $\underline{P2}$ $\underline{P3}$ $\underline{P4}$ $\underline{P5}$ $\underline{P6}$

Stop Code

Cd = P1 P2 P3 P4 P5 P6

Code Delete

Sk = K $\underline{P5}$ $\underline{P6}$

4-bit Control Character
Inhibit entrance of Control Characters in 4-bit

Tpa	=	Pp	P1
		Output gate	P1 bit

Tpb	=	Pp	P2
		Output gate	P2 bit

Tpc	=	Pp	P3
		Output gate	P3 bit

Tpd = Pp P4

Output gate P4 bit

Tpe = Pp P5

Output gate P5 bit

Tpf = Pp P6

Output gate P6 bit

Tpa = Xp

Tpb = Xp

Tpc = Xp

Tpd = Xp

Tpe = Xp

Tpf = Xp