Section 4

Maintenance

SECTION IV

MAINTENANCE

4.1 GENERAL

The maintenance procedures used on the LGP-21 Computer System follow standard electronic practice. Special instructions and equipment are necessary only for the memory section (magnetic disc). The memory unit maintenance instructions are supplied in Sections 4.6.1 and 4.6.2. Special tools and/or equipment may be obtained from the Commercial Computer Division, Parts Department.

The mechanical maintenance for the Flexowriter, Tally Reader, and Tally Punch is covered in the respective manuals. The Tally Reader Manual and the Tally Perforator Manual are included in Sections VIIA and VIIB of this publication. The modified FL Flexowriter, which is used with this system, is basically the same (mechanically) as the units used with previous systems. The mechanical maintenance for the Flexowriter has been covered in the Flexowriter Adjustment Manual, which all field personnel should now have.

4.2 FLEXOWRITER ELECTRO-MECHANICAL CIRCUIT DESCRIPTIONS

The following circuit descriptions explain the electro-mechanical action, in sequence, for the circuits involved. All relay and switch contacts refer to schematic (L543 002 008) in Section VI.

4.2.1 Automatic Carriage Return

For purposes of explanation, assume the Flexowriter to be finishing a program-controlled tabulation. The existing conditions are LKL dropped, KFB dropped, and SCRT transferred (Figure 4-1a). The carriage operated contacts SF4 and SF1 break between contacts 3-2 and 3-4 respectively. At this time the tab stop engages the tab lever, operating the unlatch mechanism which restores SCRT. KFB is prevented from energizing by contacts 4-3 of SF1 which are still open. Contacts 1 and 2 of SF4 now make, followed immediately by contacts 1 and 2 of SF1. This allows KOC to energize.

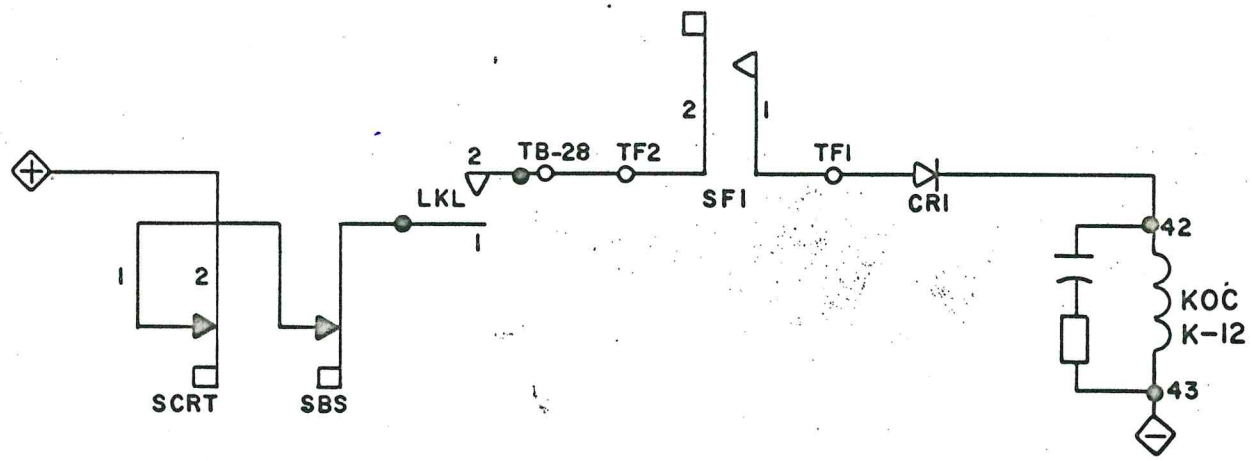


FIGURE 4-1(a) AUTOMATIC CARRIAGE RETURN

When KOC picks, KACR then picks. KFB is prevented from picking by KOC's N/C contacts 24 and 25 (Figure 4-1b).

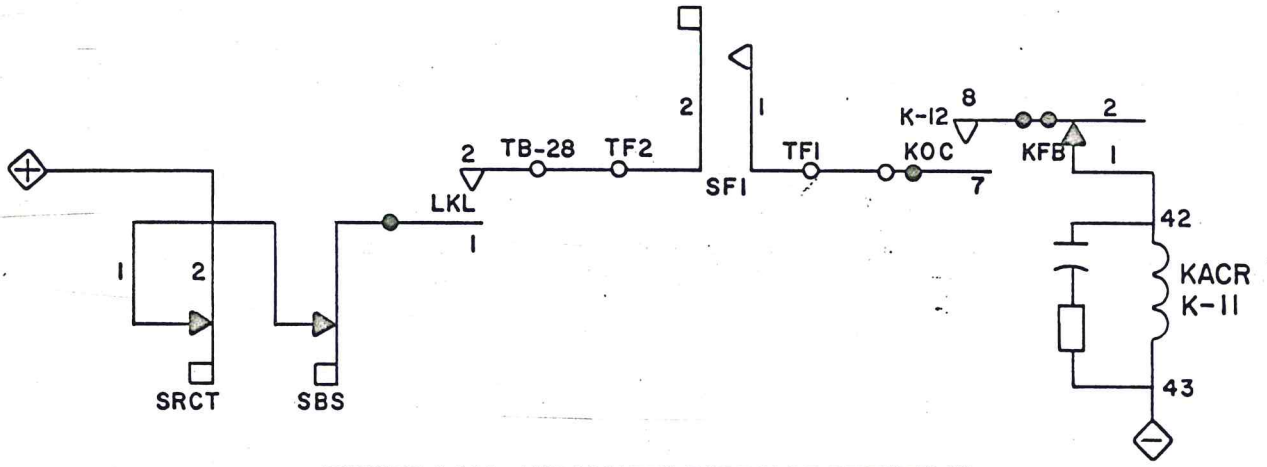


FIGURE 4-1(b) AUTOMATIC CARRIAGE RETURN (Cont.)

When KACR picks, translator action is initiated as follows: the carriage return code is applied to the ranslator by energizing LT4 and the translator clutch. The circuit for this is shown in Figure 4-1c.

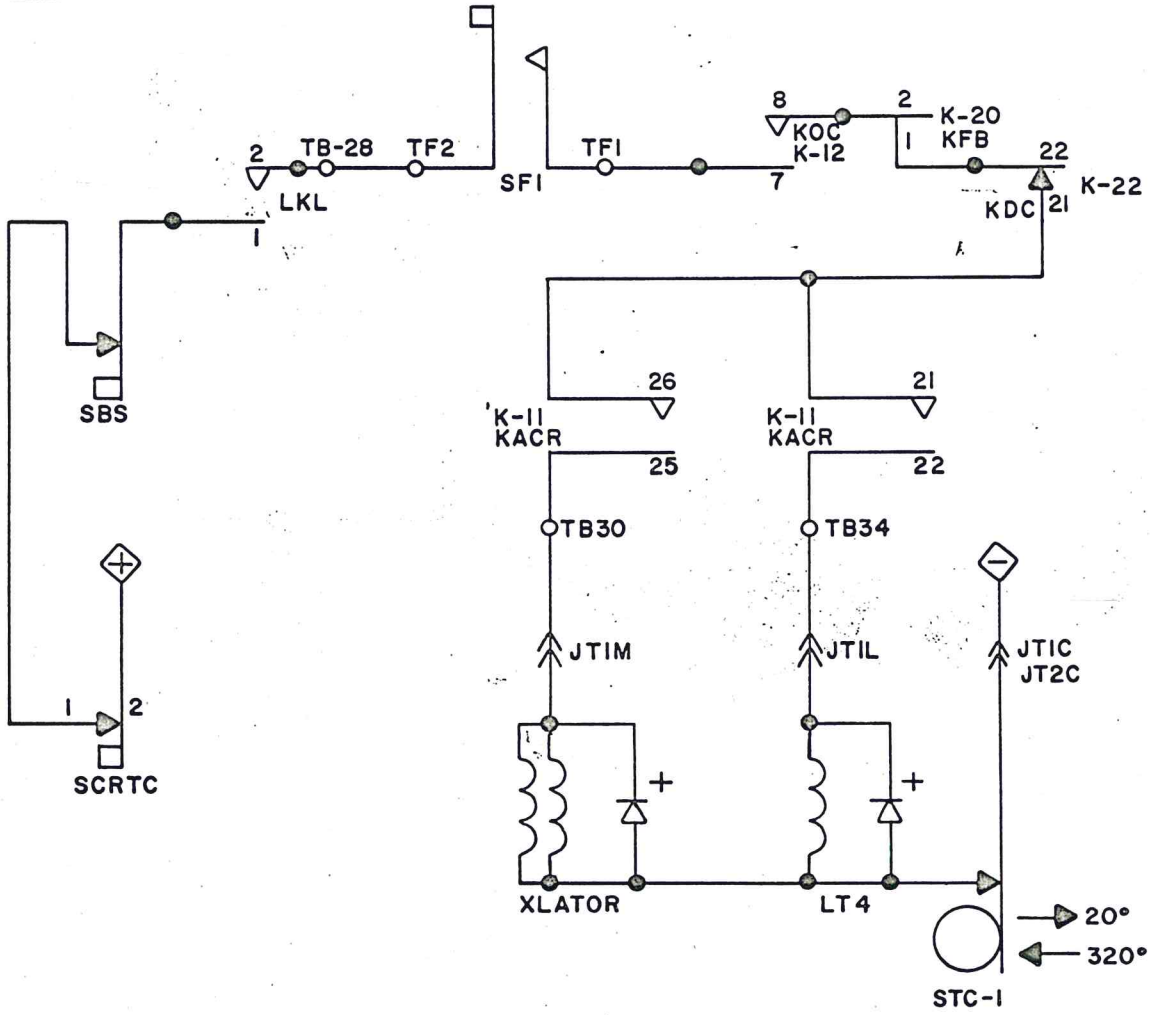


FIGURE 4-1(c) AUTOMATIC CARRIAGE RETURN (Cont.)

The clutch now energizes, and the translator begins its cycle with LT4 (CR) energized.

At 20 degrees of the translator cycle, cam operated STC-1 transfers energizing KCRI. Through its time delay circuitry KCRI will hold for 100 ms after STC-1 is restored (Figure 4-1d.) This breaks the energizing path for the translator magnets and inhibits the reader until after the carriage return function is completed.

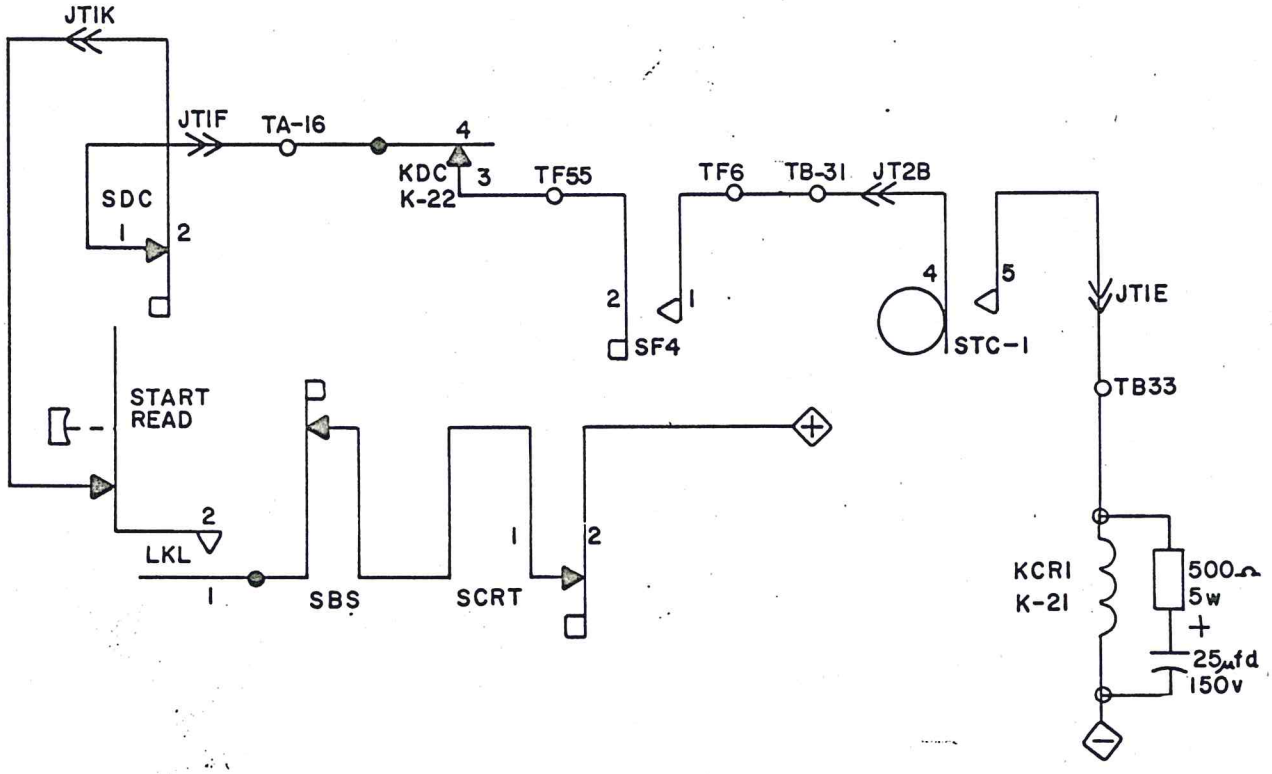


FIGURE 4-1(d) AUTOMATIC CARRIAGE RETURN (Cont.)

When the carriage return key is pulled, it operates a bail which in turn transfers SDC, energizing KDC (K22). (See Figure 4-1e).

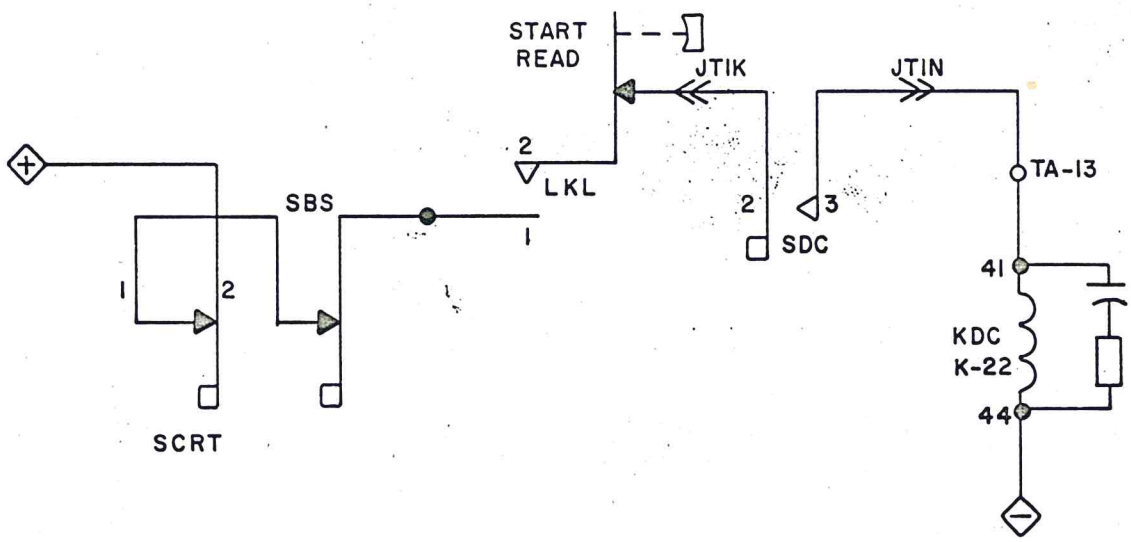


FIGURE 4-1(e) AUTOMATIC CARRIAGE RETURN (Cont.)

SDC is immediately restored with the operation of the Carriage Return key. However, KDC has now established a hold path as shown in Figure 4-1f.

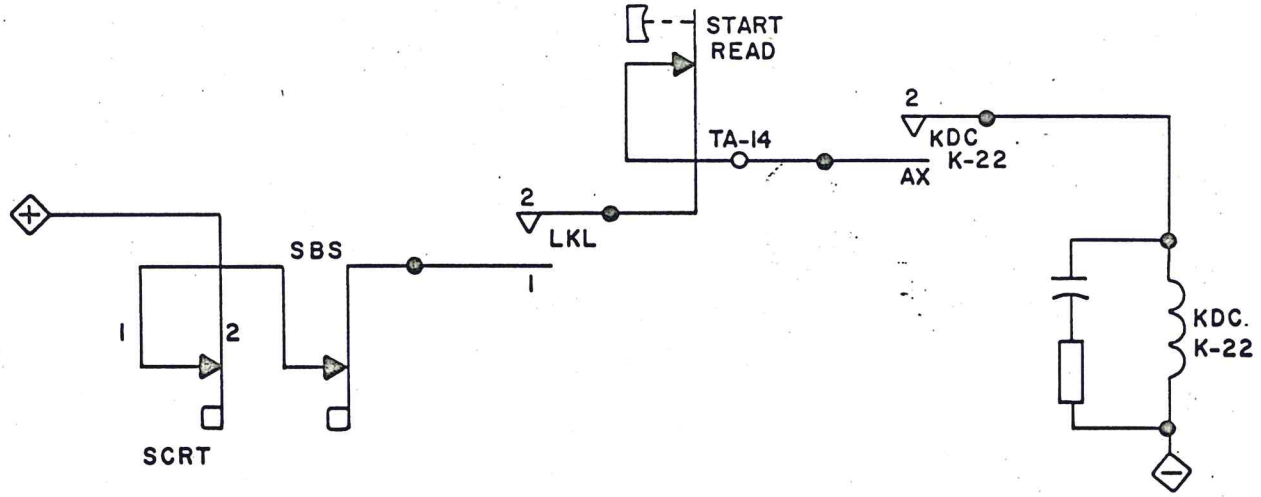


FIGURE 4-1(f) AUTOMATIC CARRIAGE RETURN (Cont.)

As the Carriage Return key operates, punching (if punch is ON) of the CR code is inhibited by KACR, which was energized and held as described earlier. KACR N/C contacts 28 and 27, through which the punch clutch and code magnet energizing current must pass, are held open during the translator cycle, thus inhibiting the punch during an automatic carriage return. Late in the translator cycle, SCRT transfers, dropping out LKL and KDC. KFB remains dropped out due to KACR N/C Contacts 5 and 6 and KCRI N/C Contacts 1 and 2. KRCI remains energized (100 ms delay). KACR is now held as shown in Figure 4-1g.

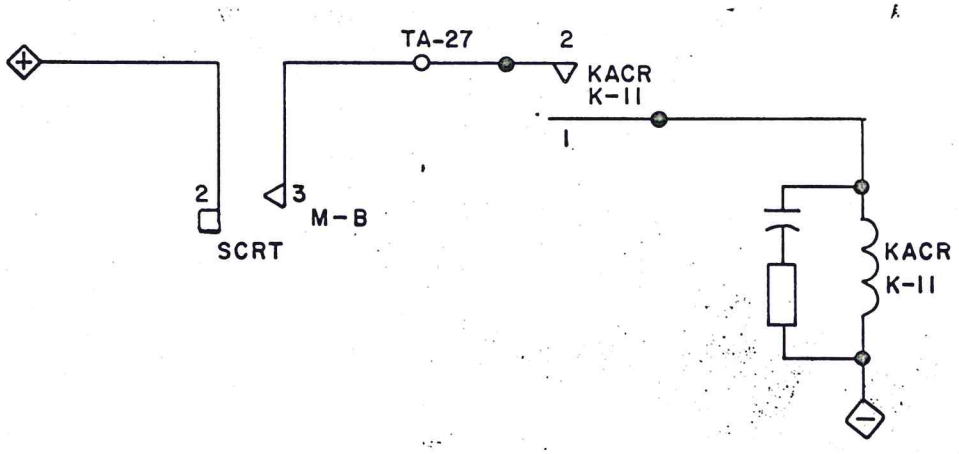


FIGURE 4-1(g) AUTOMATIC CARRIAGE RETURN (Cont.)

KACR holds for the duration of the CR operation. At the time of the SCRT transfer, the CR clutch energizes and winds up the CR tape causing SF1 and SF4 to return to their normal positions. Neither can have any effect, however, until KACR and SCRT are restored.

4. 2. 2 Program-Controlled Carriage Return Operation

At T3 (sign time) of phase 1 of a Print instruction, LTC and LT4 in the translator are energized by their respective storage drivers, Tx and Tp-2 and the translator begins to operate, pulling down the CR seeker. A projection on the seeker contacts a bail (same for Tab and BS seekers) which causes SDC (delay control switch) to transfer. This will pick the delay control relay K-22, dropping out the feed back relay, K-20. Contacts 5-6 of KFB open. KFB must remain de-energized until CR, Tab, or BS function has been completed. If the computer comes to another Print instruction before the CR, Tab, or BS is completed, JL-33 must remain false (controlled by KFB 5-6). Thus the computer will stop in blocked state phase 1 and wait until KFB restores at end of control function. As stated before, when SDC transfers, contacts 1-2 break causing immediate drop-out of KFB. When SDC 2-3 make, KDC picks and insures that KFB will stay dropped by breaking KDC 3-4. At this point, SDC is restored. KDC is held through 1-2 of the normally closed SCRT contacts. Further into the translator cycle, the actual CR or Tab operation is performed by the respective cam tripping against the power roll. As a result, the SCRT re-establishes the energizing circuit for KFB (by re-energizing LKL) at the termination of the CR or Tab operation. The computer is now allowed to proceed; i. e. , X can come true because JL-33 is now true. The above sequence is identical for BS operation except that SBS operates instead of SCRT.

4. 2. 3 Punch Error Relay Operation

During the process of punching a tape, it is desirable to have an indication of incorrect operation. In the systems Flexowriter used in the LGP-21, this is accomplished by the relay KPE (K3) which will lock the keyboard and inhibit the reader. When a character is typed, transferring the SC contacts, SCC transfers. This picks the code magnets and the clutch magnet as shown in Figure 4-2a.

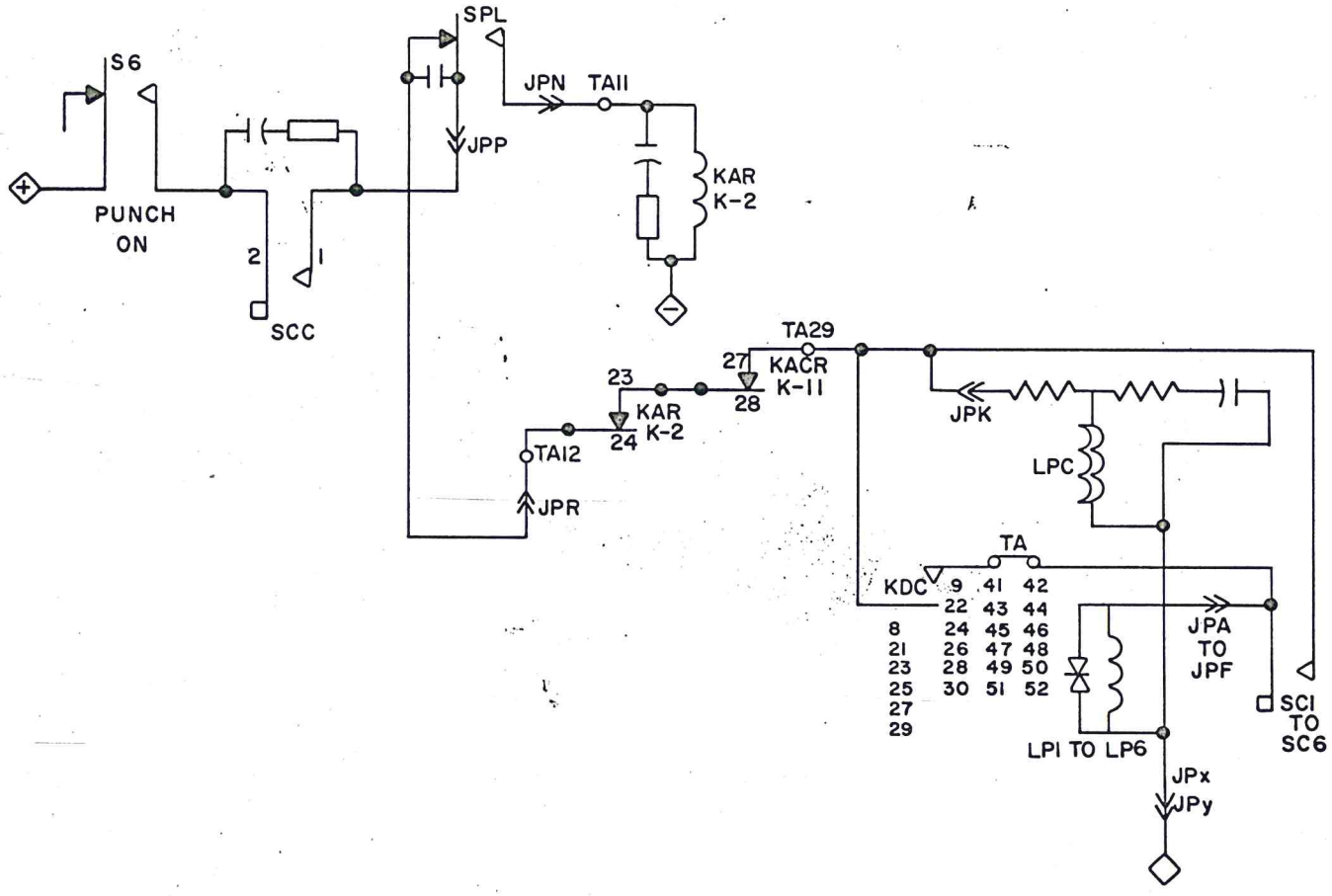


FIGURE 4-2(a) PUNCH ERROR RELAY OPERATION

SPL transfers, breaking the path for current flow through the punch magnets and picking KAR. KAR will hold through the circuitry shown in Figure 4-2b until the SCC contacts restore.

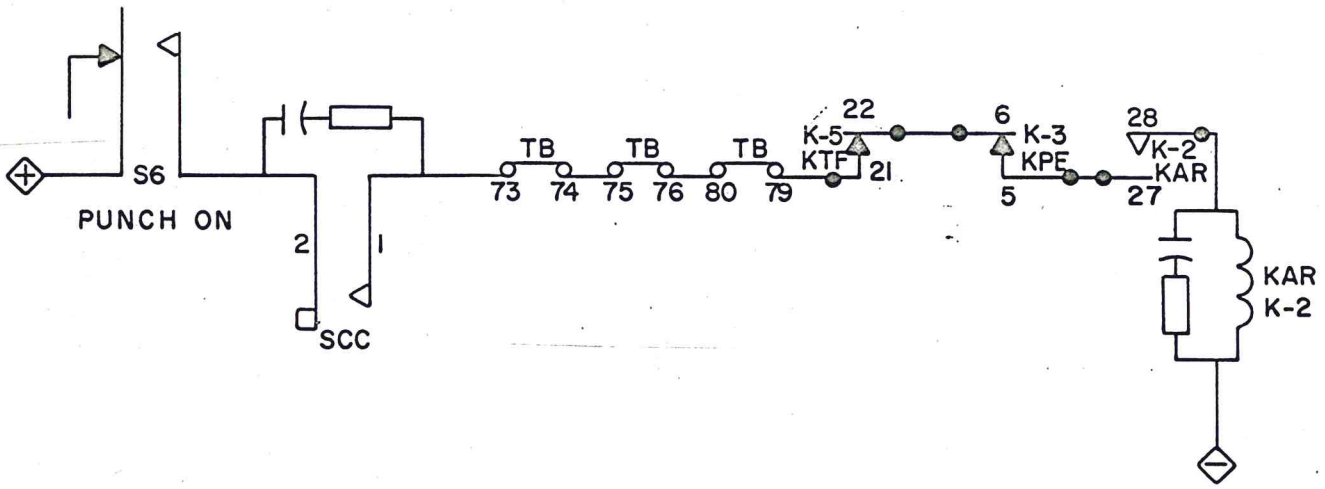


FIGURE 4-2(b) PUNCH ERROR RELAY OPERATION (Cont.)

If SCC stays transferred for longer than the normal time because of sluggish selector slides, jammed selector slides, or characters typed manually so that one type bar follows the previous one too closely, KAR will hold long enough to pick KPE as shown below (Figure 4-2c).

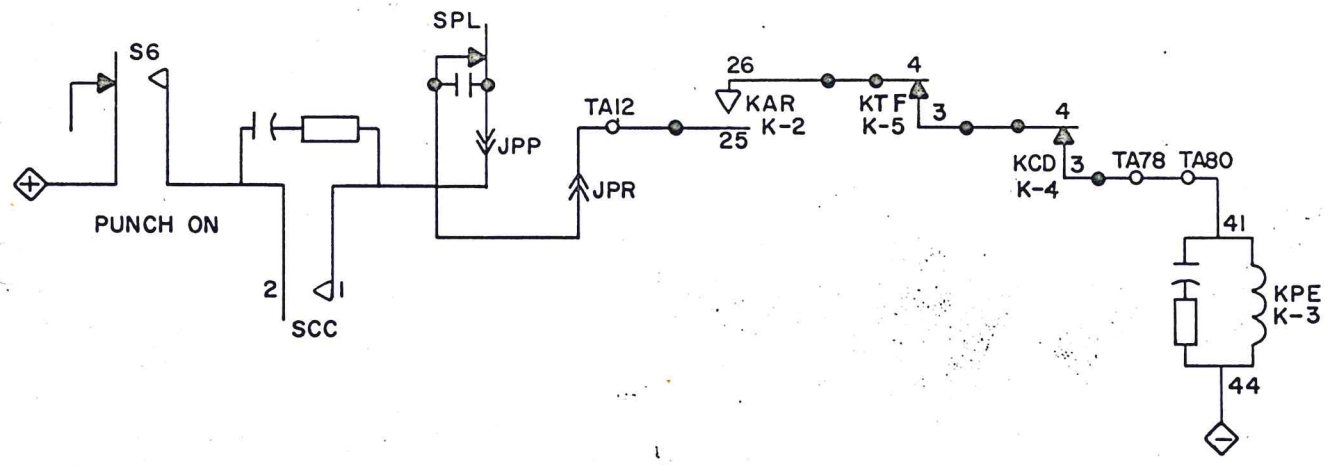


FIGURE 4-2(c) PUNCH ERROR RELAY OPERATION (Cont.)

KPE will hold (Figure 4-2d) until the hold path is broken by depressing the Code Delete lever which picks KCD, thereby dropping KPE and restoring normal operation.

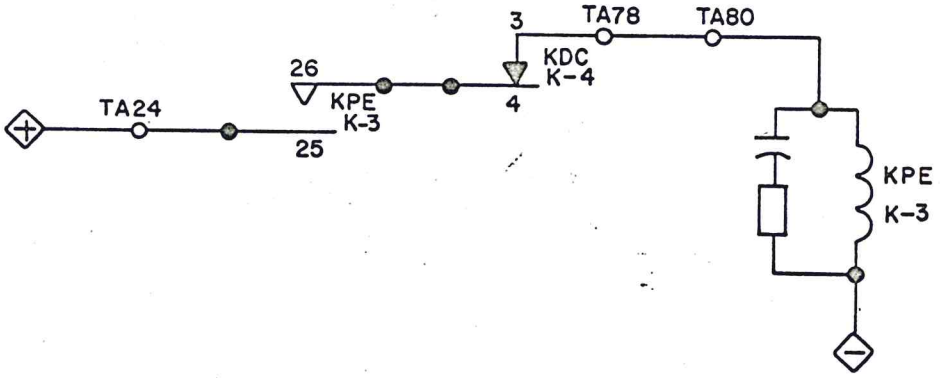


FIGURE 4-2(d) PUNCH ERROR RELAY OPERATION (Cont.)

If the tape in the punch jams, runs out, or is subjected to excess tension, it is possible to pick KPE by operating the SPT contacts as shown in Figure 4-2e. KPE holds as shown above and requires a Code Delete to restore normal operation.

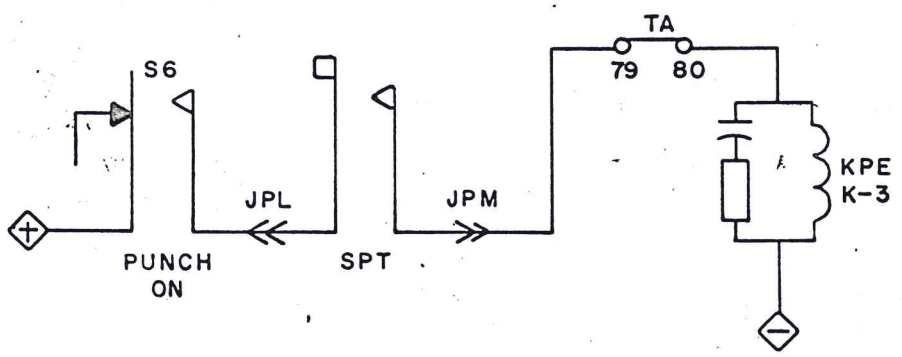


FIGURE 4-2(e) PUNCH ERROR RELAY OPERATION (Cont.)

It can easily be seen that pulling in KPE during a malfunction opens KPE's normally closed contacts 3 and 4, which will drop LKL, thus locking the keyboard. Dropping LKL also interrupts the pick circuit for the reader clutch (LR) and the Manual Input Light, due to LKL's normally open contacts 1 and 2.

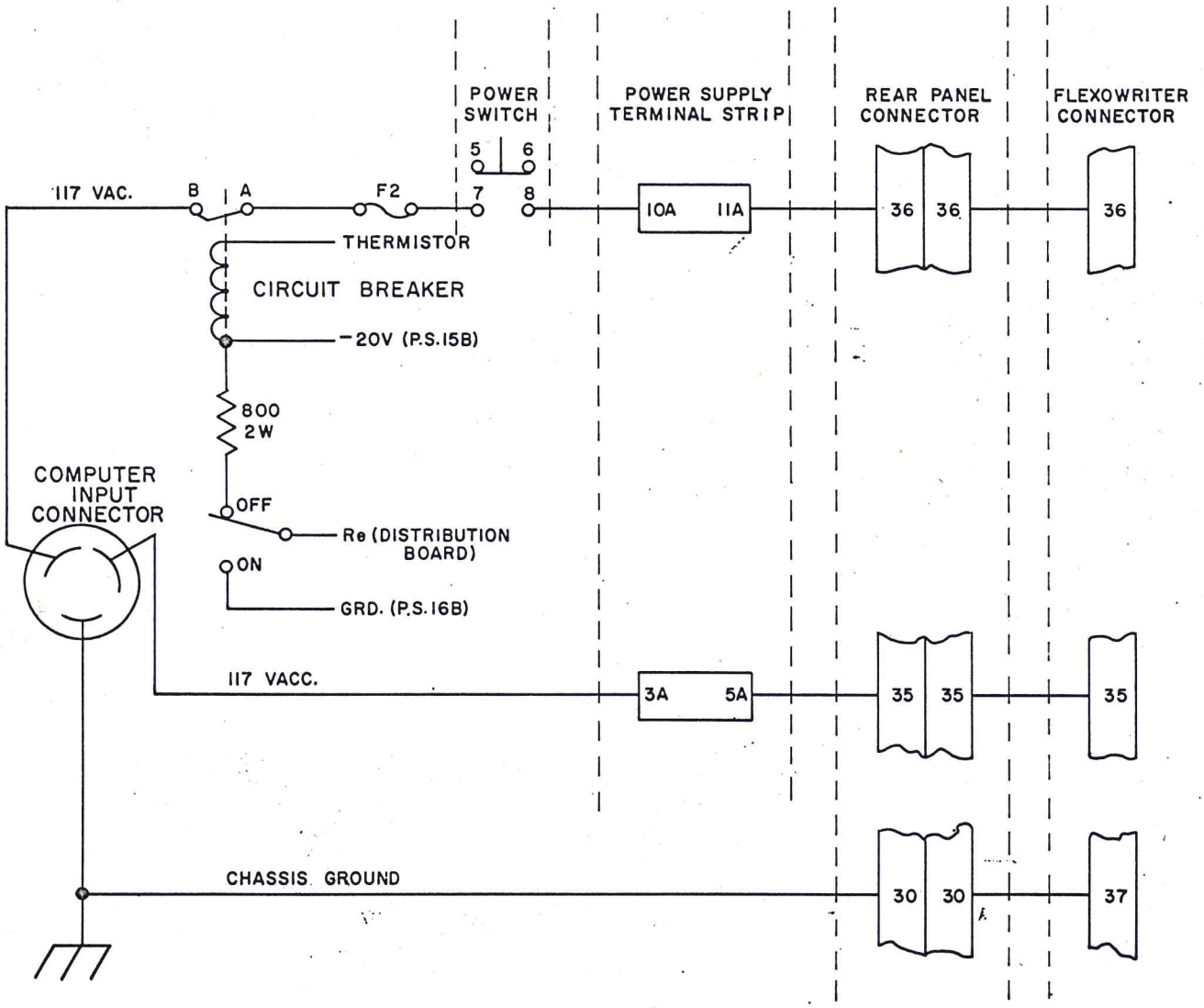


FIGURE 4-3 A. C. POWER TO FLEXOWRITER

4. 3 FLEXOWRITER RELAY CONTACT LOCATION

The following information is included to assist in minimizing service time on the electrical portion of the Flexowriter and should be used in conjunction with the parts of Sections IV, V, and VI which deal with the Flexowriter electrical schematics. The contacts used on the Flexowriter relays are grouped into three general types or forms and are defined in Figure 4-4.

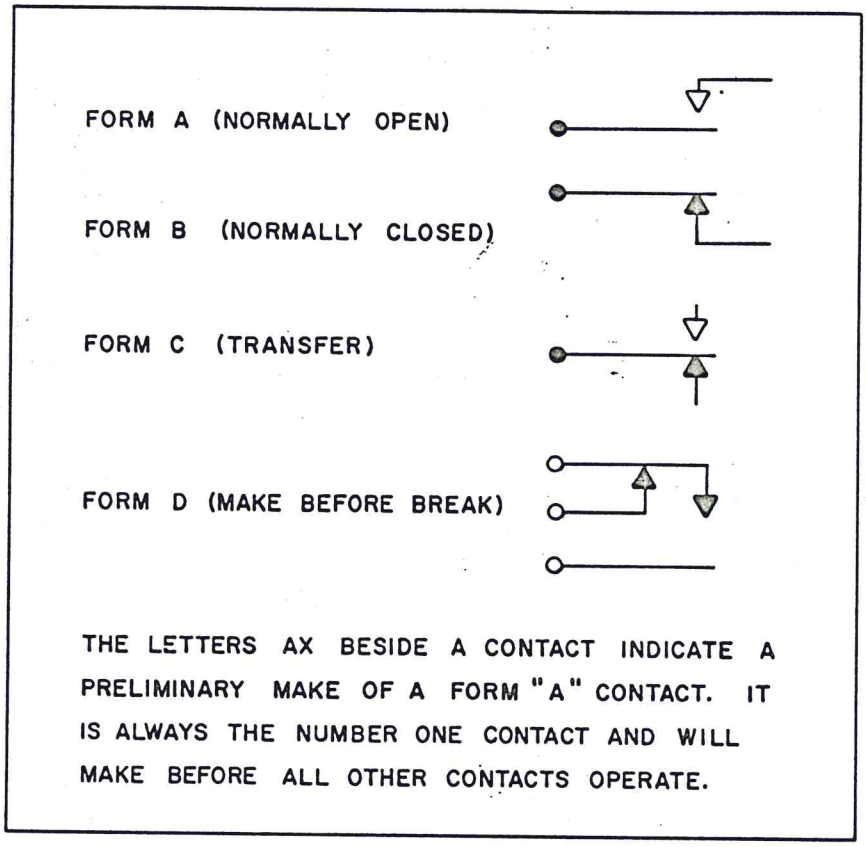


FIGURE 4-4 RELAY CONTACT CONFIGURATION

The following relay diagrams (Figures 4-5a - m) are shown in top view and facing so that the operating strap movement is toward the top of the page. All relays are shown unoperated. Figures 4-6a - c show the locations of the contacts.

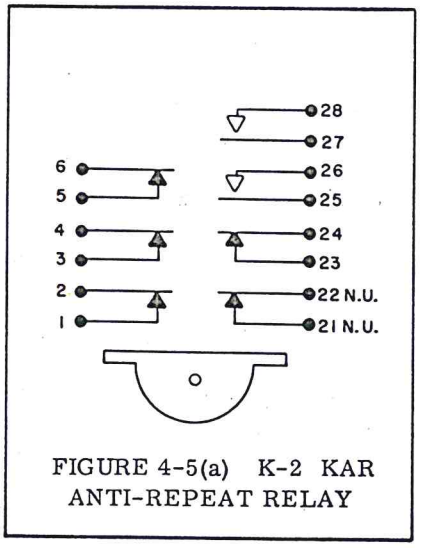


FIGURE 4-5(a) K-2 KAR ANTI-REPEAT RELAY

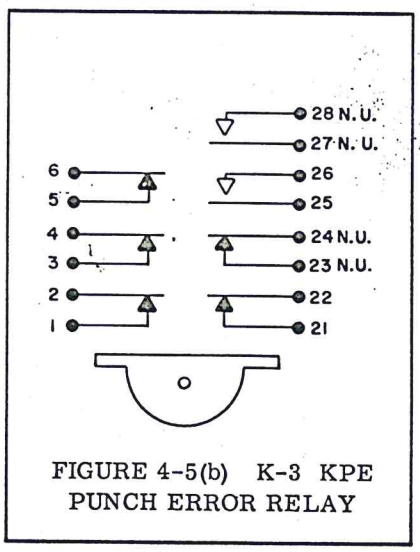


FIGURE 4-5(b) K-3 KPE PUNCH ERROR RELAY

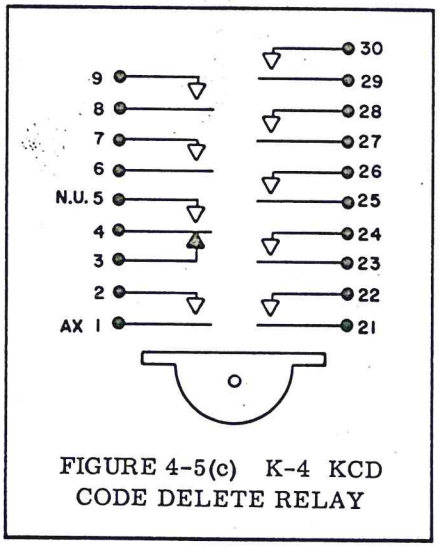


FIGURE 4-5(c) K-4 KCD CODE DELETE RELAY

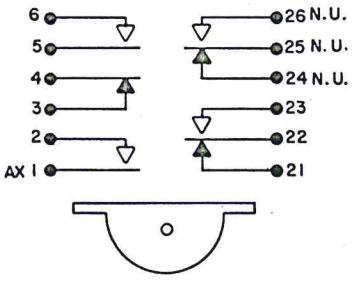


FIGURE 4-5(d) K-5 KTF TAPE FEED RELAY

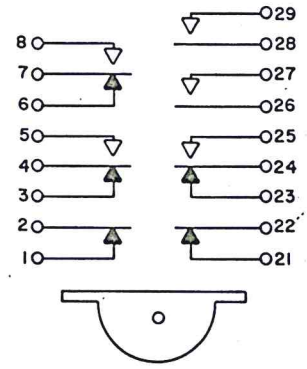


FIGURE 4-5(e) K-10 KCF CARD FEED (Used only in Flexowriter Incorporating Card Reader)

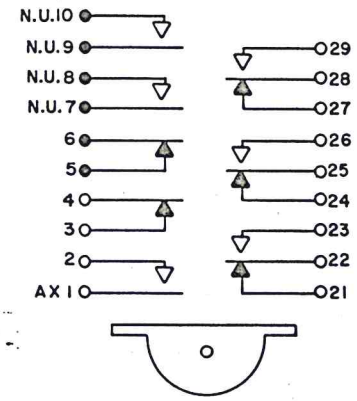


FIGURE 4-5(f) K-11 KACR AUTOMATIC CARRIAGE RETURN RELAY

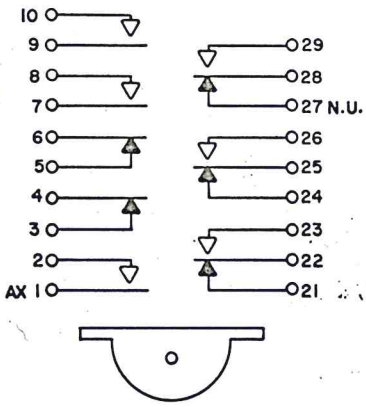


FIGURE 4-5(g) K-12 KOC OUTPUT CONTROL RELAY

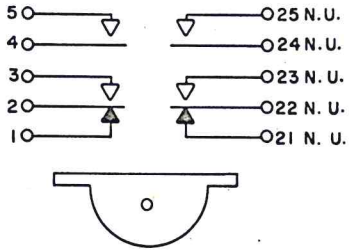


FIGURE 4-5(h) K-15 KMI MANUAL INPUT RELAY

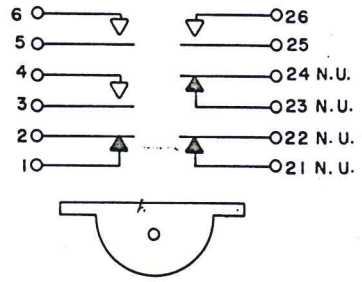


FIGURE 4-5(j) K-20 KFB FEED BACK RELAY

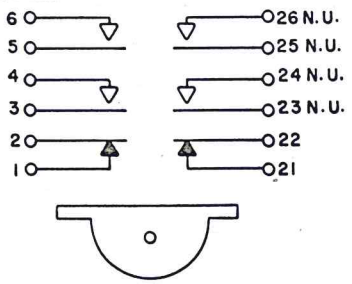


FIGURE 4-5(k) K-21 KCRI CARRIAGE RETURN INTERLOCK RELAY (100 ms DROPOUT +25 MS

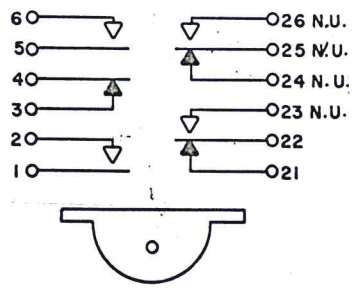


FIGURE 4-5(m) K-22 KDC DELAY CONTROL RELAY

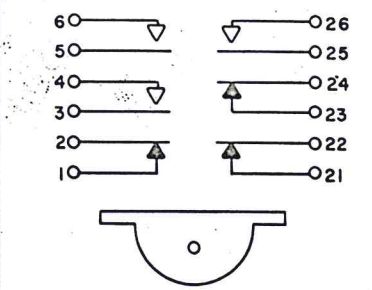


FIGURE 4-5(n) K-23 KRC READ CONTROL RELAY

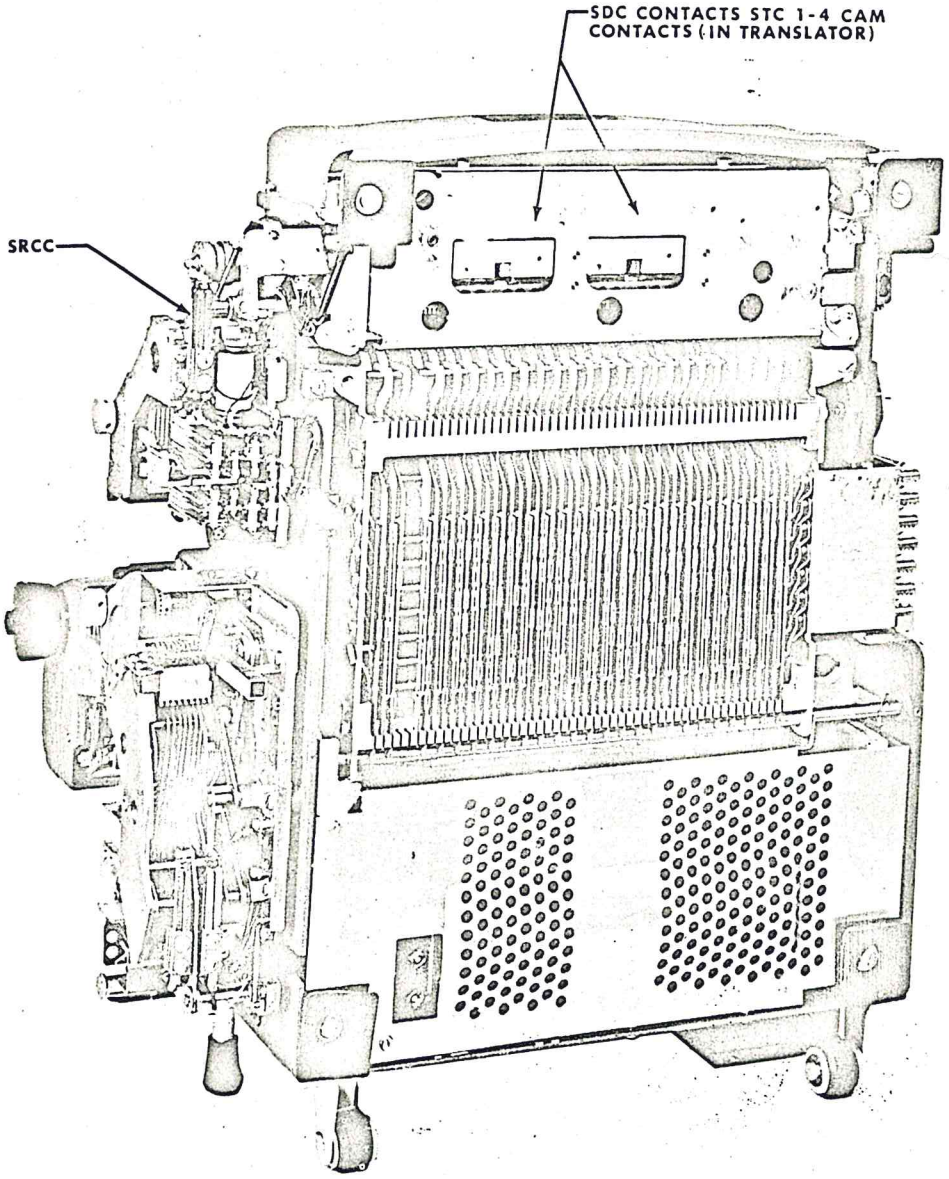


FIGURE 4-6(a) SWITCH CONTACT LOCATIONS

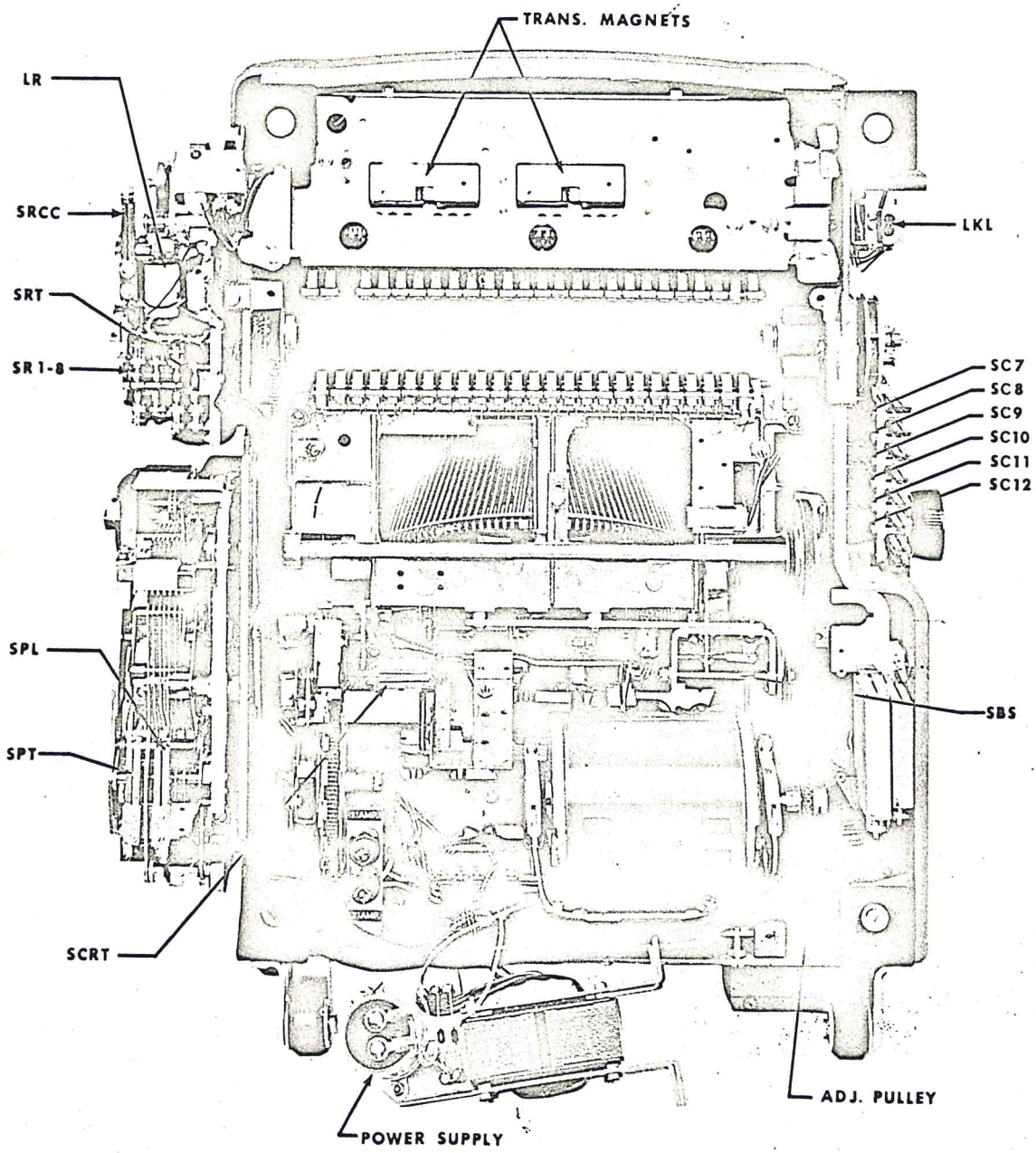


FIGURE 4-6(b) SWITCH CONTACT LOCATIONS (Cont.)

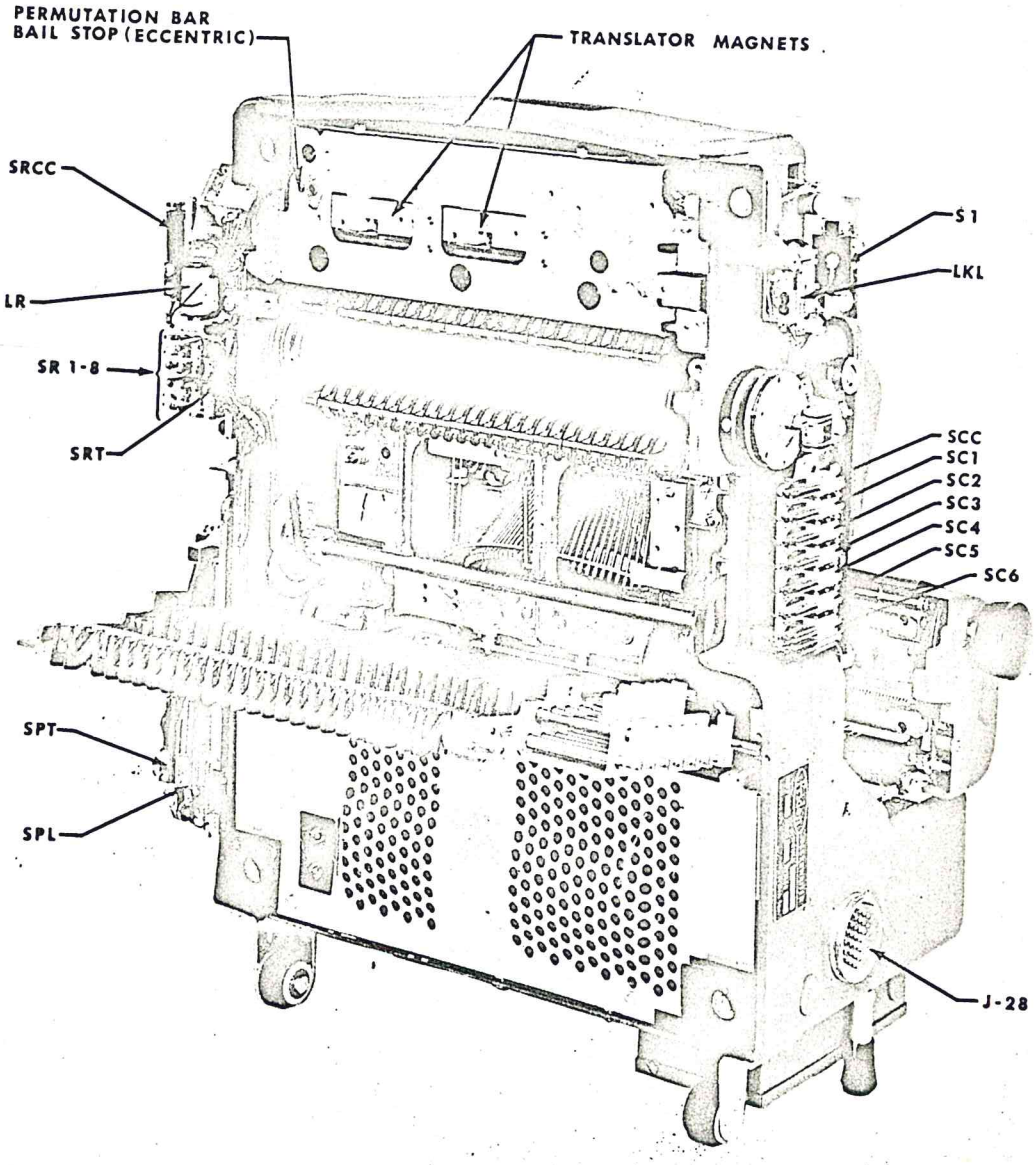


FIGURE 4-6(c) SWITCH CONTACT LOCATIONS (Cont.)

4.4 FLEXOWRITER ELECTRICAL MAINTENANCE SPECIFICATIONS

The electrical timing relationships and adjustment specifications should be checked during installation and preventive maintenance.

4.4.1 Selector Contact Adjustment (SC)

Adjustment of SC7 through 12 and the form "C" contact of SC6 is critical. All form "C" contacts must break before make, and SC7 must make after all other form "C" contacts make.

4.4.2 Cam-Operated Contact Adjustment (STC)

SRCC, Form B: Must break after SRC makes and make before SRC breaks.

STC-1, Form B: Tungsten - Break 20 degrees; make 320 degrees.
Form C: Transfer 20 degrees, restore 320 degrees.

STC-2, Form A: Make 10 degrees, break 350 degrees.
Form B: Break 10 degrees; make 350 degrees.

STC-3, Form C: Transfer 260 degrees; restore 300 degrees.

STC-4, Form C: Transfer 250 degrees; restore 310 degrees.

When adjusting STC contact timing, check the timing with a meter at JT plugs after setting clutch. Timing should agree within ± 3 degrees and allow a minimum of .010" contact overtravel.

4.4.3 Reader Contact Adjustment (SR)

Straps 1, 2, and 3 of SRC and SR 1-6 must break before make.

Straps 4 and 5 of SR1 and 6 must make before straps 4 and 5 of SR 2 and 5 break.

Straps 4 and 5 of SRC must make before SRCC breaks.

Straps 6 and 7 of SRC should be set to .020" maximum gap.

4.4.4 Field Switch Adjustment - Automatic Carriage Return (SF)

Adjust the field switch so that there is no contact motion one space before, or after, the switch-operating arm contacts the actuators. The field switch contacts should have a minimum of .010" overtravel when transferred.

4.4.5 Timing and Mechanical Flow Charts

See figures 4-7 and 4-8.

4.5 POWER SUPPLY

The following tests cover the power distribution and switching specifications for the computer.

4.5.1 Operating Parameters and Tolerances

No Load Test:

1. The voltage supplied at the +15v, -15v, -20v, and the -20dv terminals shall not be

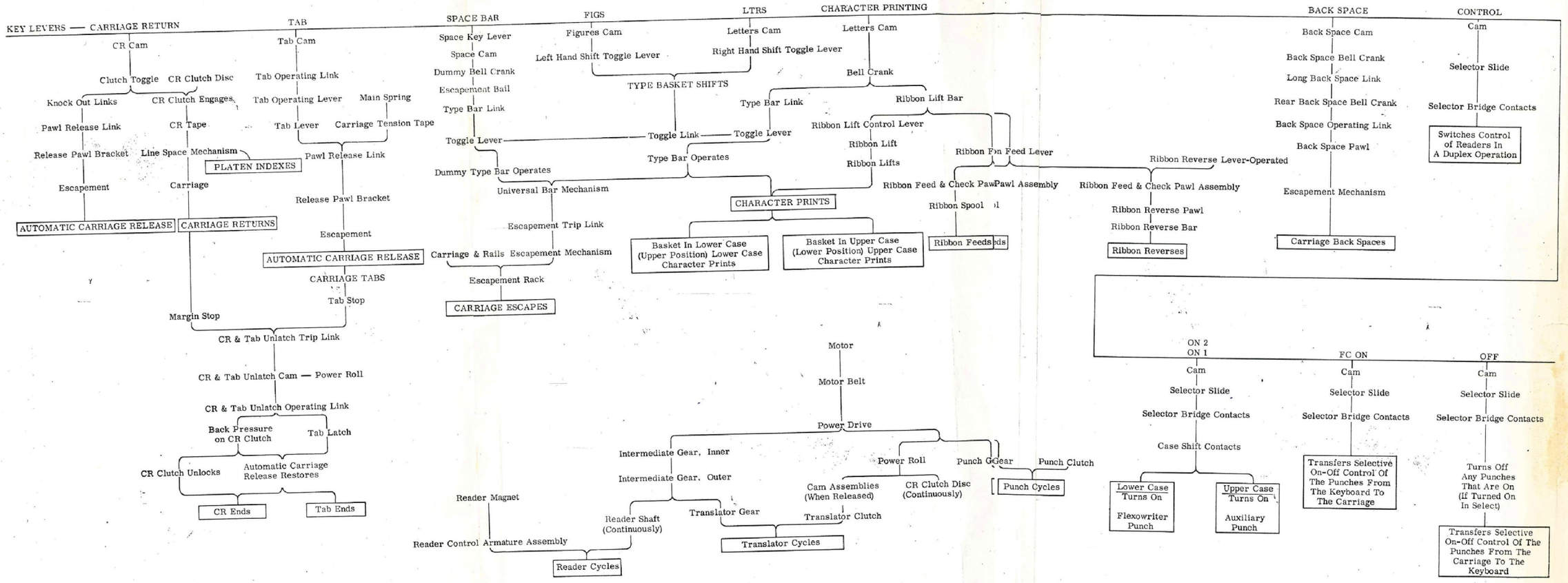
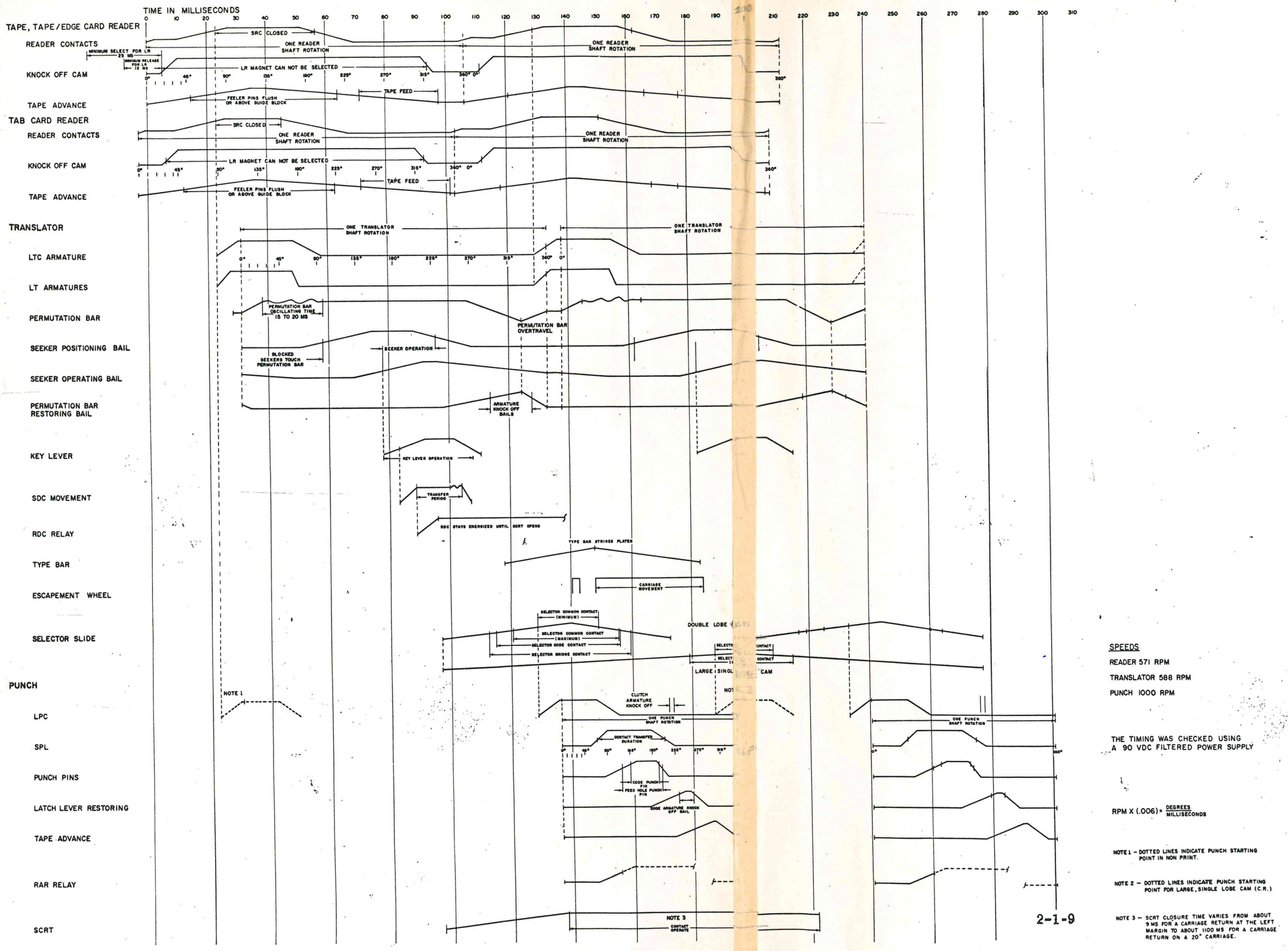


FIGURE 4-7 FLEXOWRITER FLOW CHART



SPEEDS

READER 571 RPM

TRANSLATOR 588 RPM

PUNCH 1000 RPM

THE TIMING WAS CHECKED USING A 90 VDC FILTERED POWER SUPPLY

RPM X (.006) = $\frac{\text{DEGREES}}{\text{MILLISECONDS}}$

NOTE 1 – DOTTED LINES INDICATE PUNCH STARTING POINT IN NON PRINT.

NOTE 2 – DOTTED LINES INDICATE PUNCH STARTING POINT FOR LARGE, SINGLE LOBE CAM (C.R.)

NOTE 3 – SCRT CLOSURE TIME VARIES FROM ABOUT 9 MS FOR A CARRIAGE RETURN AT THE LEFT MARGIN TO ABOUT 1100 MS FOR A CARRIAGE RETURN ON A 20" CARRIAGE.

FIGURE 4-8 FLEXOWRITER TIMING CHART (AVERAGE VALUES)

more than 15% above rated voltage.

2. Ripple shall be less than 3/4v peak to peak.

Half Load Test

1. The voltage supplied at the −15v, -15v, -20v, and the -20dv terminals shall be within a ± 10% tolerance.

2. Ripple shall be less than 3/4v peak to peak.

4. 5. 2 AC Verification

Step 1 Remove fuses (F1, F2, F3) from the rear panel and insert power cord from 115v line into the input connector. Using a Triplett V. O. M., check for 115v AC at the accessory connectors and at the power supply modulok (between terminals 3A and 6A and between terminals 3A and 10A). No voltage should be found.

Step 2 Turn interlock OFF. Insert fuses (F1, F2, F3). Verify that 115v AC is now present at the accessory connectors. Depress POWER switch. It should be impossible to turn ON the power indicator with the interlock OFF.

Step 3 In order to seat the circuit breaker correctly, it is necessary that the POWER switch be OFF when the interlock is turned ON. Turn ON the interlock and wait 30 seconds to see if the power indicator comes ON. If it does not, depress the POWER switch. Should the POWER switch have already been ON, depress it to turn power OFF and then reset the circuit breaker by throwing the interlock OFF and ON. Depress the POWER switch. Verify that the power indicator and stop indicator are illuminated.

Step 4 Verify that 115v AC exists between modulok terminals 3A and 6A and between modulok terminals 3A and 10A.

Step 5 Depress the POWER switch (power indicator should go out) and repeat Step 4. This time no voltage should be found.

4. 5. 3 Ground Test

Step 1 With the power off, use the V. O. M. to measure continuity between the computer chassis and

a. P. S. modulok terminal 16A.

b. Each of the two points labeled ground on the distribution board.

c. Pin 34 in the display connector.

d. Pin A in the J1 connector.

4. 5. 4 Supply Voltage Test

Step 1 With the power ON, use the V. O. M. to measure +15v between the computer chassis and

a. P. S. modulok terminal 18A.

b. P. S. modulok terminal 18B.

c. The point labeled +15v on the distribution board.

d. Pin Y in the J3 connector.

e. Pin 3 in the display connector.

Step 2 With the power ON, use the V. O. M. to measure -15v between the computer chassis and

a. P. S. modulok terminal 17A.

b. P. S. modulok terminal 17B.

c. The point labeled -15v on the distribution board.

d. Pin W in the J3 connector.

e. Pin 4 in the display connector.

Step 3 With the power ON, use the V. O. M. to measure -20v between the computer chassis and

a. P. S. modulok terminal 15A.

b. P. S. modulok terminal 15B.

c. The point labeled -20v on the distribution board.

d. Pin Z in the J3 connector.

e. Pin 2 in the display connector.

Step 4 With the power ON use the V. O. M. to measure -20v (-20v delay) between the computer chassis and

a. P. S. modulok terminal 14A.

b. P. S. modulok terminal 14B.

c. The point labeled -20d on the distribution board.

d. Pin B in the J1 connector.

e. Pin 32 in the display connector.

5. 5 Switch Test

Step 1 With the power OFF place all Breakpoint Switches in the OFF position. Place the Transfer Control switch in the ON position. Place the MODE switch in the One Operation position. With a V. O. M. verify continuity between the computer chassis and

a. Points Tc, tb1, tb2, tb3, tb4, bq, O1, be, TO and bs on the distribution board.

b. Point be on the distribution board only when the EXECUTE button is depressed.

c. Point bs on the distribution board only when the START button is depressed.

d. Point bq on the distribution board only when MODE switch is in the Manual Input position.

e. Point O1 on the distribution board only when the MODE switch is in the Normal position.

f. Point Re on the distribution board only when the Record Enable switch is in the ON position.

Step 2 With the power OFF, and a V. O. M. on the R X 1000 scale, measure between chassis and

a. Point brc on the distribution board; depress the FILL CLEAR switch and observe a change in resistance.

b. Point brc on the distribution board, depress the FILL CLEAR switch and observe a change in resistance in an opposite direction from that noted in (a) above.

Step 3 With the power ON, place all Breakpoint Switches in the ON position. Place the Transfer Control switch in the OFF position and the MODE switch in the One Operation position. With a V. O. M. verify that -20v (± 10%) appears between the computer chassis and

a. Points Tc, tb1, tb2, tb3, tb4, bq, O1, be and bs on the distribution board.

b. Point be on the distribution board only when the EXECUTE button is depressed.

c. Point bs on the distribution board only when the START button is depressed.

d. Point bq on the distribution board only when the MODE switch is in the Manual Input position.

e. Point O1 on the distribution board only when the MODE switch is in the Normal position.

f. Point T0 on the distribution board only when the I/O switch is depressed.

4. 5. 6 Motor Start Relay Adjustment Procedure

This procedure is given below in three steps, with references to points shown in Figure 4-9.

Step 1 When in the de-energized position, the armature of the motor start relay must be adjusted so that an air gap of no greater than 3/16" exists between it and the coil form. Under this condition the armature must also allow the contacts to remain closed and provide only minimum clearance at point B.

Step 2 With the armature in the energized position (armature held against coil form), the contact must be open and a gap of 1/8" should exist between the armature and its support bracket at point C.

Step 3 Begin by forming the armature to provide the 1/8" gap at C with the armature held against the coil form. Then release the armature and check for proper clearance at A. Reform if necessary. Finally, check the armature to contact clearance at B and approve its operation.

4. 6 DISC AND MEMORY HEAD MAINTENANCE PROCEDURES

The maintenance procedures for the main memory section are contained herein. At this point, the specifications and adjustments are considered preliminary. When additional information is received, a correction, supplement, or Field Information Notice (FIN) will be issued.

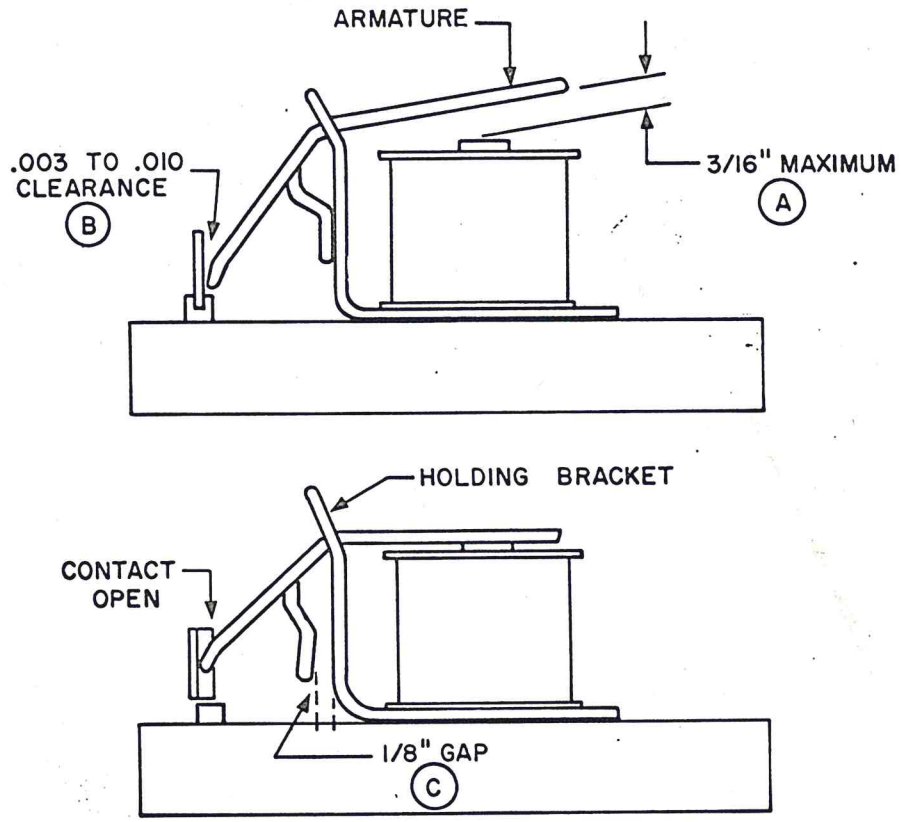


FIGURE 4-9 MOTOR START RELAY ADJUSTMENTS

NOTE: Heads are measured with high gain differential amplifier with no bias loads or circuitry.

4. 6. 1 Main Memory Head Specifications

Heads will be classified according to readback voltage:

Class 1 Heads with readback between 340 to 380 mv. will be acceptable for use on all tracks of memory and are identified by a GREEN dot.

Class 2 Heads with readback between 380 to 400 mv. will be acceptable for use on all tracks of memory except the outermost track on each head block and are identified by a RED dot.

Class 3 Heads with readback between 320 to 340 mv. will be acceptable for use on all tracks of memory except the innermost track on each head block and are identified by a YELLOW dot.

Main memory readback signals, measured at the output of the main memory preamplifier (Vrh), shall be between 6. 0 volts and 12. 0 volts peak-to-peak. This shall apply to all main memory heads, including spares.

The relationship of the clock to the main memory readback signal (Vrh) shall be acceptable for all bits if it is as shown in Figure 4-10.

There may be some phase shift between the readback signal (Vrh) and the clock. Maximum allowable phase shift is as shown in Figure 4-11.

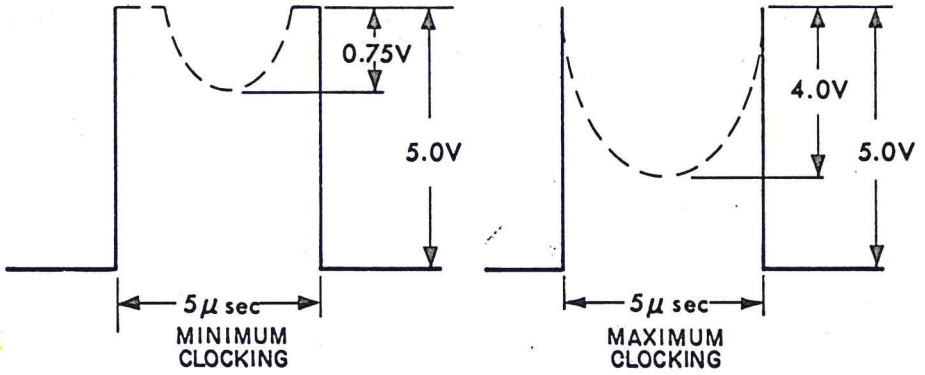


FIGURE 4-10 RELATIONSHIP OF MAIN MEMORY READBACK SIGNAL AND CLOCK PULSE
(Measured at the collector of Q57 on memory control card)

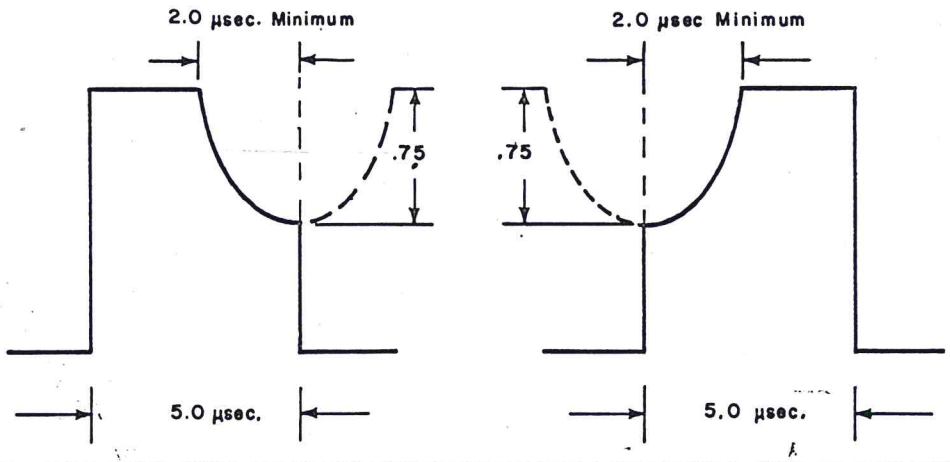


FIGURE 4-11 RELATIONSHIP OF MAIN MEMORY READBACK SIGNAL AND CLOCK PHASE SHIFT
(Measured at the collector of Q57 on memory control card)

The width of the clock signal (negative clock), measured at Cp, shall be between 4.5 and 5.0 μsec.

4.6.2 Main Memory Head Replacement and Adjustment Procedure

When replacing a head in the LGP-21 memory, the following procedure should be used:

Step 1 Stop the disc. Remove the main memory head access cover plate and the mounting screws for the memory matrix board assembly. Back off the head pressure adjusting screw for the defective head, until the main memory head reed raises above the two head-mounting studs.

Step 2 Lift out the defective head and tilt back the memory matrix board assembly to gain access to the electrical connections on the bottom of the board. Unsolder the leads of the defective head.

Step 3 Refer to Section 4.6.1 and select a replacement head. Note that the center tap connection to the coil is color coded with a red tip and will be attached to the terminal connection, while the coil ends will be attached to the diodes. Solder in the replacement coil. Do not use excessive heat when soldering the leads to the diodes.

Step 4 Place the new head on the disc surface and align the head mounting studs with the holes in the reed.

Step 5 Turn the head pressure adjusting screw clockwise until the tip of the reed just comes in contact with the shoe, on the head. See Figure 4-12.

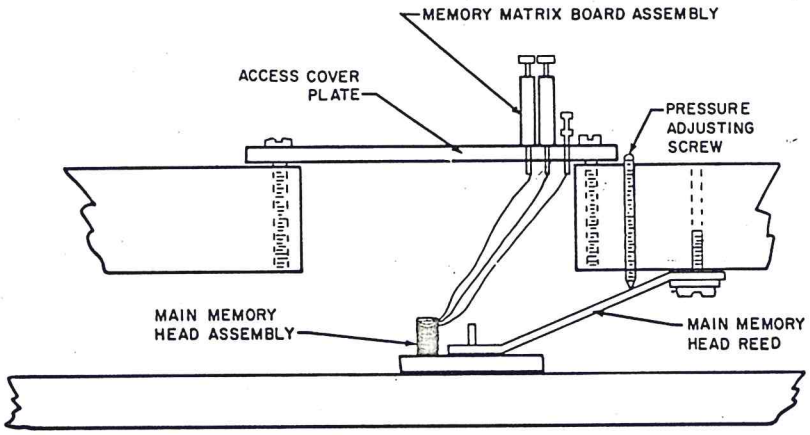


FIGURE 4-12 MAIN MEMORY HEAD REPLACEMENT

NOTE: This is a critical point and can be determined accurately by viewing the downward travel of the reed, while the adjusting screw is being turned.

Step 6 At this "point of contact," the head adjusting screw should be turned an additional 170 degrees for any of the five inside heads to produce the required 6 ± 1 grams pressure.

For any of the four outside heads, on each of the head blocks, the head adjusting screw should be rotated 140 degrees after the "point of contact" for the required 5 ± 1 grams pressure. See Figure 4-13

When these steps are accomplished, information should be recorded into the location where the new head has been installed and the playback should be checked. If the playback is within the limits specified in section 4. 6. 1, the new head is acceptable. If the playback is not within these limits, recheck the adjustments or replace the head if necessary. This method of adjustment has been devised to allow for pressure and playback considerations.

NOTE: Excessive pressure should never be used to increase the playback signal, as the heads must fly free of the disc coating when operating. Excessive pressure has resulted in damaging the disc coating.

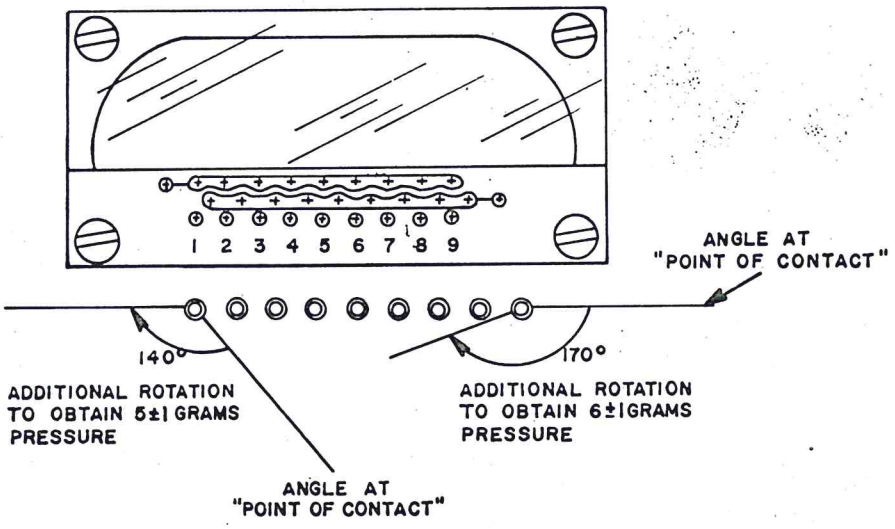


FIGURE 4-13 MAIN MEMORY HEAD ADJUSTMENT

4. 6. 3 Recirculating Register Specifications

The recirculating register readback signals shall be saturated in the positive-going portion of the signal. The amplitude of the signal, when saturated, shall be between 10v and 14v, as seen in Figure 4-14.

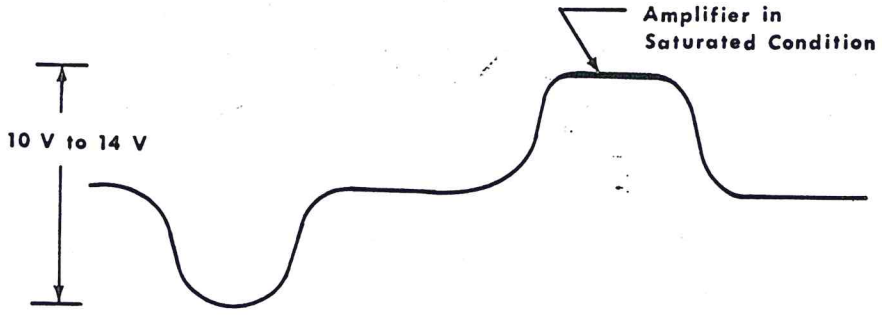


FIGURE 4-14 RECIRCULATING REGISTER READBACK SIGNAL

The relationship of the clock to the recirculating line readback signals shall be acceptable if it is as shown in Figure 4-15, when looking at the point where the 680 pf clocking capacitors, the 2. 4K resistors, and the base input diodes are connected.

Where there is jitter in the readback, the clock shall be set so that it clocks at the most positive point, as shown in the "Minimum" figure..

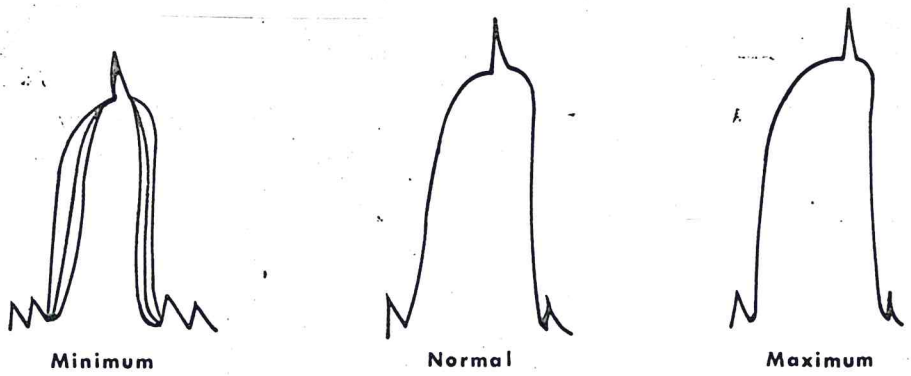


FIGURE 4-15 RECIRCULATING REGISTER CLOCK

The interaction factor for each of the recirculating registers is measured as follows:

> The register under observation shall be filled whenever possible with a pattern of all zeros. The other registers shall be filled whenever possible with alternating 1's or 0's or with H's. The modulation of the register under observation shall be less than 1 volt peak-to-peak when measured at the output of the read amplifier.

4. 6. 4 Recirculating Register Head Adjustment Procedure

It has been found that, while the recirculating registers are reliable in themselves, there is a tendency toward electrical interaction between individual registers. This is due to the fact that all the recirculating heads are tracking at nearly the same physical distance from the center of the disc. Slight variations in head adjustment may cause the read station of the head to sense electromagnetic flux changes which have

been recorded by one or more of the other registers. The following procedure may be used to minimize the effects of this interaction.

Step 1 Clear one of the registers and enter an alternate bit pattern in the others (FFFFFFFF).

Step 2 Observe the readback of the cleared register at the output of its read amplifier (Xrh), which is located on the memory control board. Any interaction between the cleared register and any of the other registers will manifest itself as variations in the base line of the cleared register. These variations should not exceed an amplitude of one volt (peak-to-peak).

Step 3 If the peak-to-peak variations exceed one volt, a radial adjustment may be made to move the head out of the field of interference. However, it must be remembered that moving any of the recirculating heads along the radius of the disc will affect the relationship of the pattern being recirculated and the clock pulses being applied to the data amplifier. Care must be taken to be sure that the head is not moved so far as to interrupt normal recirculation. Several adjustments may be necessary to obtain the most optimum clock pulse position with the least amount of interference from the other registers. If the interference cannot be adjusted to less than one volt peak-to-peak, a new head should be installed.

Step 4 To adjust the remaining registers, repeat steps 1, 2, and 3 for each of the other registers.

Step 5 After all the registers have been adjusted, it will be necessary to recheck each one to ascertain that the adjustments made last have not re-introduced interference in the registers which were adjusted first. Repeat steps 1 through 5 until all registers are correct.

4.6.5 Memory Head Location and Oscilloscope Patterns

Figures 4-16 and 4-17 point out the main memory head locations and typical oscilloscope patterns, which are included as an aid in maintenance procedures.

4.7 CONVERSION OF DECIMAL TRACK-AND-SECTOR ADDRESSES TO HEXADECIMAL

The following rules explain how to convert a decimal track-and-sector address to its hexadecimal equivalent. The conversion process is in two steps; first the track portion is converted, then the sector portion.

Conversion of track portion:

Divide the track number by 8 - the quotient is the first hexadecimal digit.

Multiply the remainder by 2 - the product is the second hexadecimal digit.

If the sector portion of the decimal address is equal to or greater than 64, add 1 to the second hexadecimal digit.

Conversion of sector portion:

If the sector is equal to or greater than 64, subtract 64.

Divide the sector number by 4 - the quotient is the first hexadecimal digit.

Multiply the remainder by 4 - the product is the second hexadecimal digit.

Example: Convert the decimal track-and-sector number 31 127 to its hexadecimal equivalent.

Track 31 $31 \div 8 = 3$ r 7 First hexadecimal digit is 3.

$7 \times 2 = 14 = Q$ Second hexadecimal digit is Q.

Is sector ≥ 64? Yes

$\therefore$ Add 1 $Q + 1 = W$

$\therefore$ 3W is the desired track address.

Sector 127 $127 - 64 = 63$

$63 \div 4 = 15$ r 3 First hexadecimal digit is W.

$3 \times 4 = 12$ Second hexadecimal digit is J.

$\therefore$ WJ is the desired sector address.

Thus the decimal address 31 127 is equivalent to 3WWJ in hexadecimal.

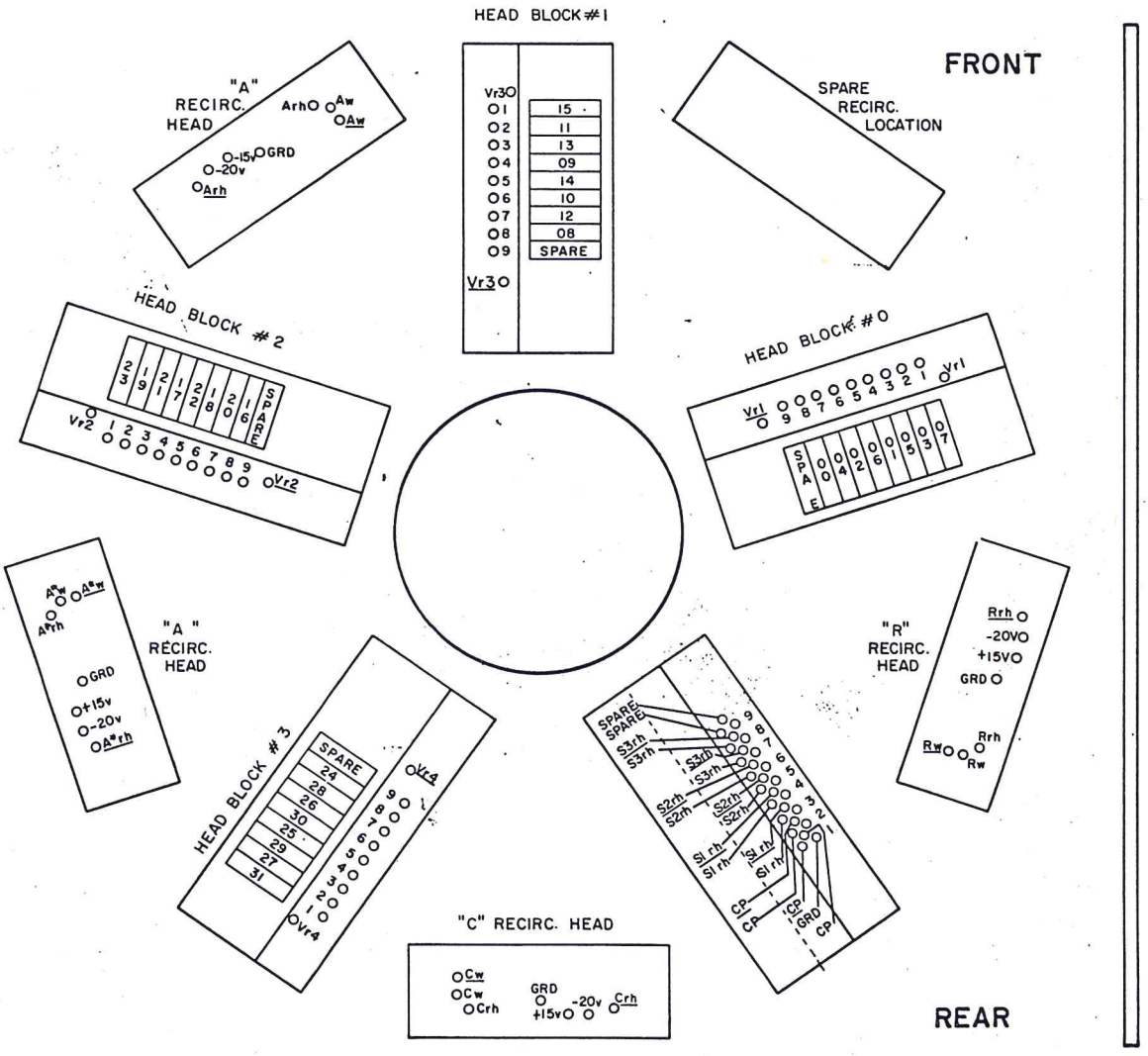
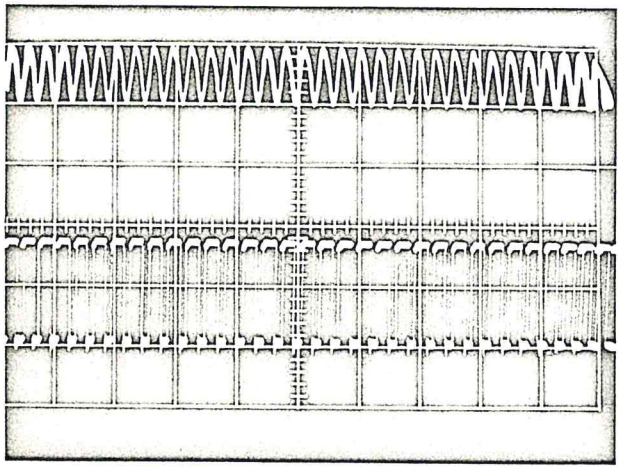


FIGURE 4-16 MAIN MEMORY HEAD LOCATIONS

Cprh

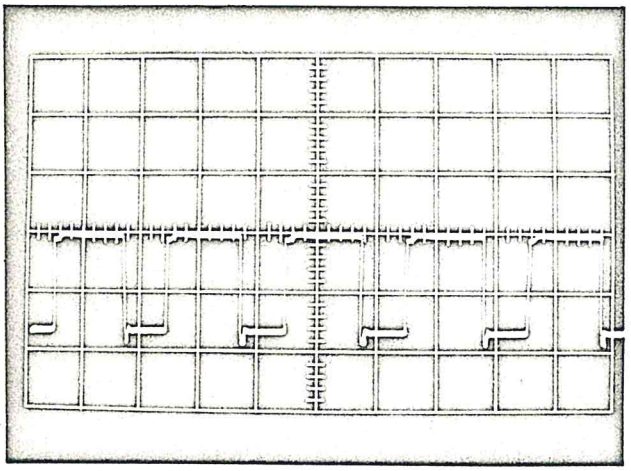
Cp



SIGNAL: ANALOG READ BACK FROM CLOCK HEAD
LOCATION: PIN 1 PLUG J-5 ON MEMORY CONTROL BOARD
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: .05 VOLTS/DIVISION NO ATTENUATION
HORIZONTAL: ONE WORD TIME

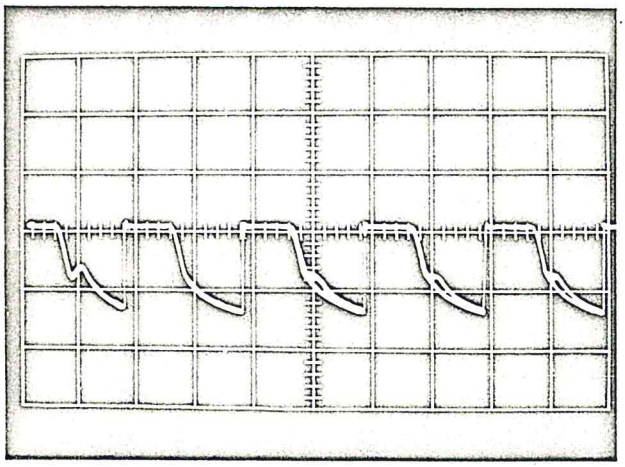
SIGNAL: OUTPUT OF INTERMEDIATE CLOCK CIRCUITRY (Cp)
LOCATION: PIN J PLUG J-3 MEMORY CONTROL BOARD
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: ONE WORD TIME

Cp



SIGNAL: EXPANDED Cp
LOCATION: SAME AS ABOVE
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: 6μSEC/DIVISION

CP

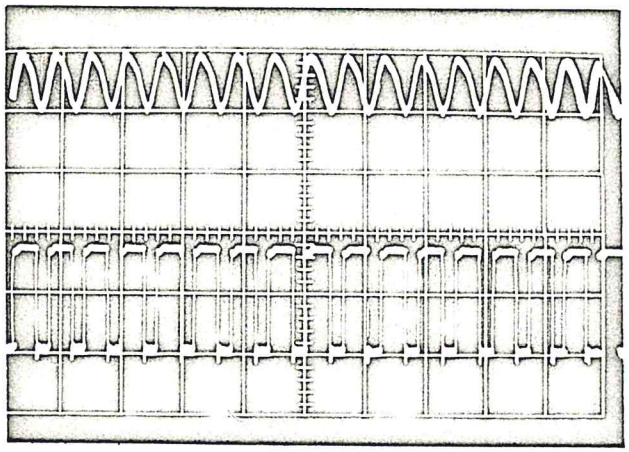


SIGNAL: OUTPUT OF CLOCK DRIVER (CP)
LOCATION: COLLECTORS OF Q105, Q107, AND Q109 ON MEMORY CONTROL BOARD. ALSO ON ALL CARDS.
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: 6 μSEC/DIVISION

FIGURE 4-17 TYPICAL SIGNALS

cprh

Cp

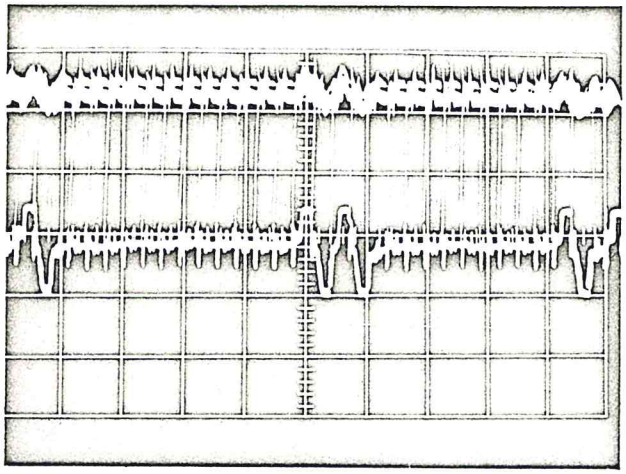


SIGNAL: READ BACK FROM CLOCK HEAD (cp)
LOCATION: PLUG J5 PIN 1
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 05 VOLTS/DIVISION, NO ATT.
HORIZONTAL: 23μSEC/DIVISION

SIGNAL: INTERMEDIATE CLOCK (Cp)
LOCATION: MEMORY CONTROL BOARD EMITTER OF Q39
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: 23 μSEC/DIVISION

arh

Arh



SIGNAL: INPUT TO "A" READ AMP
LOCATION: MEMORY DISC
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 500 MV/DIVISION
HORIZONTAL: ONE WORD TIME

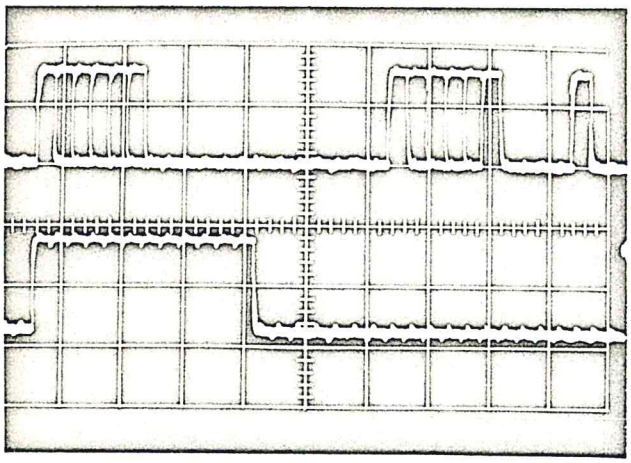
SIGNAL: OUTPUT OF "A" READ AMP
LOCATION: PLUG J2 PIN S ON MEMORY CONTROL BOARD
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 5 VOLTS/DIVISION
HORIZONTAL: ONE WORD TIME

FIGURE 4-17 TYPICAL SIGNALS (Cont.)

TIMING TRACKS

S1

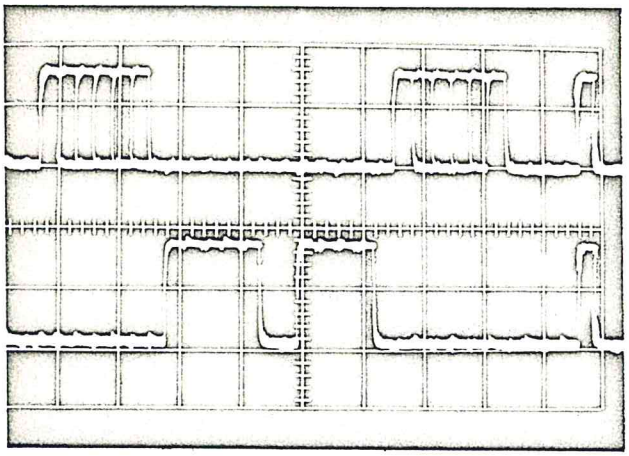
S2



SIGNAL: S1
LOCATION: MEMORY CONTROL BOARD - COLLECTOR OF Q55
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL -10 VOLTS/DIVISION
HORIZONTAL: -ONE WORD TIME

S1

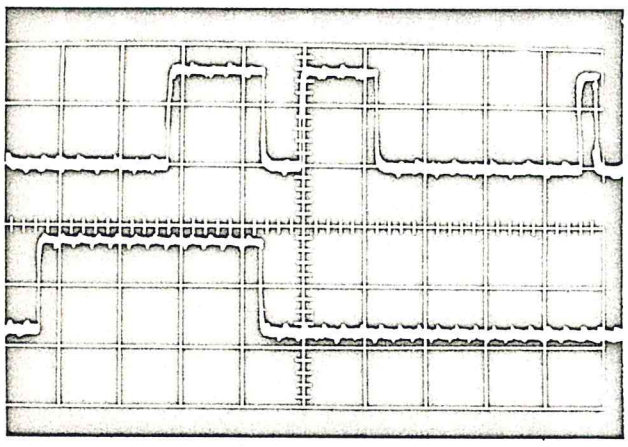
S3



SIGNAL: S2
LOCATION: MEMORY CONTROL BOARD - COLLECTOR OF Q43
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: ONE WORD TIME

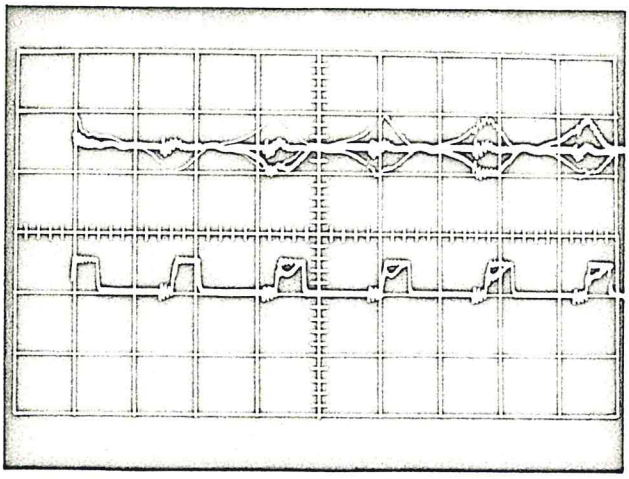
3

S2



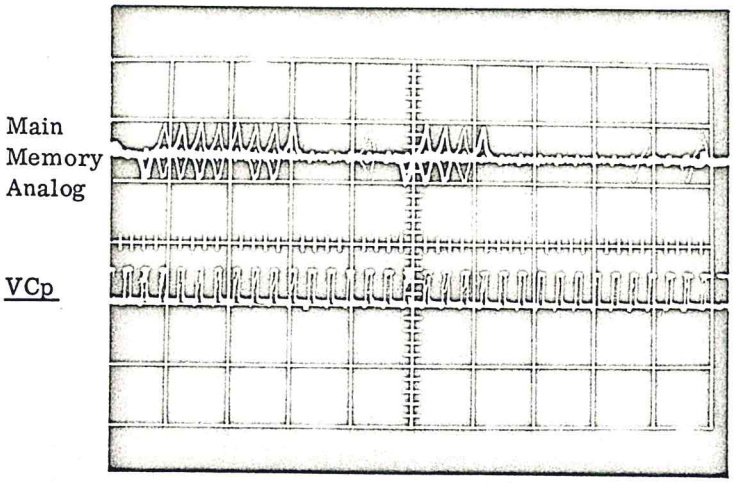
SIGNAL: S3
LOCATION: MEMORY CONTROL BOARD - COLLECTOR OF Q51
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: ONE WORD TIME

FIGURE 4-17 TYPICAL SIGNALS (Cont.)



SIGNAL: Vrh
LOCATION: MEMORY CONTROL BOARD - BASE OF Q58
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: ONE WORD TIME

SIGNAL: VCp
LOCATION: MEMORY CONTROL BOARD - COLLECTOR OF Q57
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: ONE WORD TIME

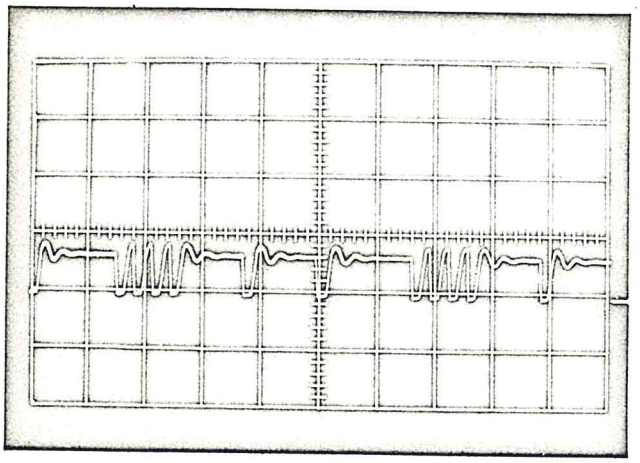


SIGNAL: Vrh
LOCATION: MEMORY CONTROL BOARD
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: 9 μSEC/DIVISION

SIGNAL: VCp
LOCATION: MEMORY CONTROL BOARD
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: 9 μSEC/DIVISION

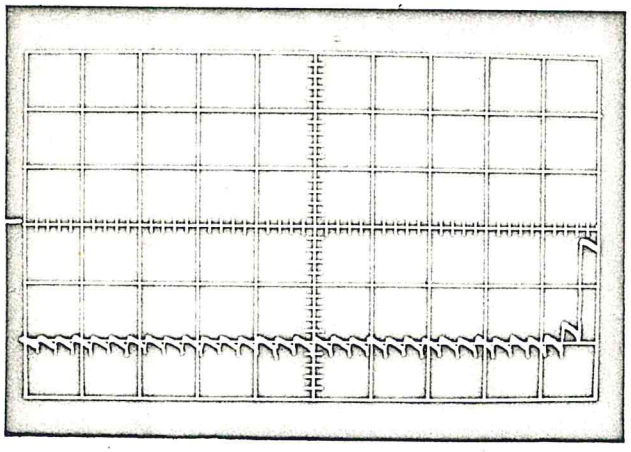
FIGURE 4-17 TYPICAL SIGNALS (Cont.)

−10 V



SIGNAL: OUTPUT OF -10V POWER SUPPLY DURING A RECORD FUNCTION
LOCATION: MEMORY CONTROL BOARD - COLLECTOR OF Q70
SYNC: POSITIVE
SYNC INPUT: W
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: ONE WORD TIME

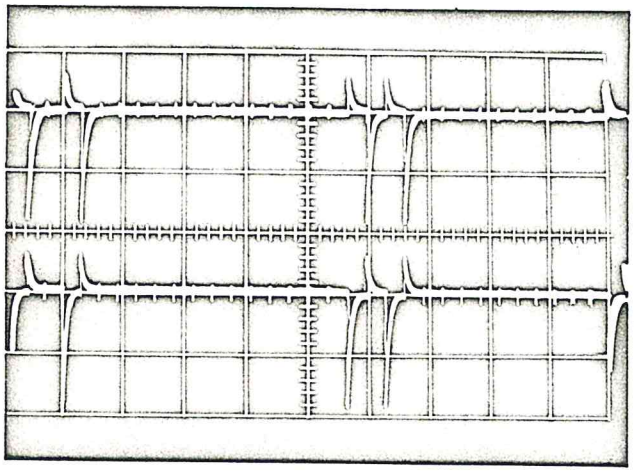
WAC



SIGNAL: WRITE AMPLIFIER CLAMP
LOCATION: MEMORY CONTROL BOARD - COLLECTOR OF Q65
SYNC: POSITIVE
SYNC INPUT: W
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: ONE WORD TIME

Aw

Aw



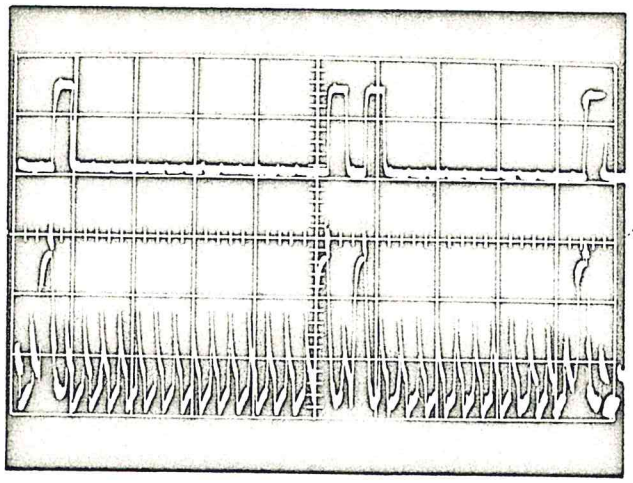
SIGNAL: Aw
LOCATION: PLUG J2-PIN Y
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: ONE WORD TIME

SIGNAL: Aw
LOCATION: PLUG J2 - PIN Z
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: ONE WORD TIME

FIGURE 4-17 TYPICAL SIGNALS (Cont.)

Ao

AI

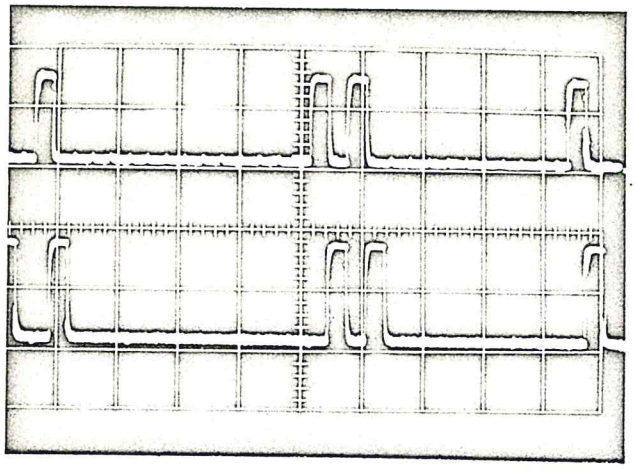


SIGNAL: OUTPUT OF THE "A" DATA AMPLIFIER
LOCATION: MEMORY CONTROL BOARD - PLUG J3 - PIN P
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: ONE WORD TIME

SIGNAL: A'
LOCATION: MEMORY CONTROL BOARD - BASE OF Q96
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: ONE WORD TIME

A

A*

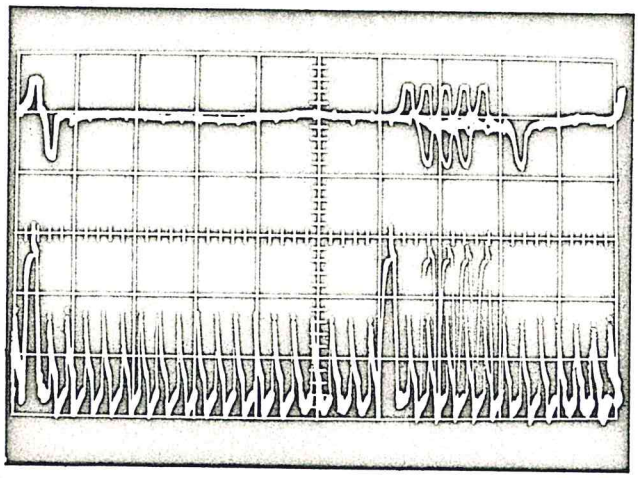


SIGNAL: OUTPUT OF "A" DATA AMPLIFIER
LOCATION: MEMORY CONTROL BOARD - PLUG J3 - PIN P
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: ONE WORD TIME

SIGNAL: OUTPUT OF "A*" DATA AMPLIFIER
LOCATION: MEMORY CONTROL BOARD - PLUG J3 - PIN S
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: ONE WORD TIME

Co

CI

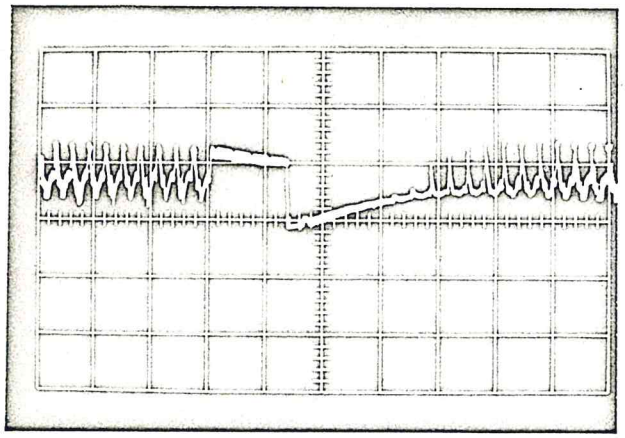


SIGNAL: OUTPUT OF "C" READ AMPLIFIER (Crh)
LOCATION: MEMORY CONTROL BOARD - PLUG J2 - PIN L
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: ONE WORD TIME

SIGNAL: C'
LOCATION: MEMORY CONTROL BOARD - BASE OF Q92
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 10 VOLTS/DIVISION
HORIZONTAL: ONE WORD TIME

FIGURE 4-17 TYPICAL SIGNALS (Cont.)

Open Head



SIGNAL: MAIN MEMORY HEAD WHICH HAS OPENED
LOCATION: CENTER TAP OF HEAD
SYNC: NEGATIVE
SYNC INPUT: T3
VERTICAL: 400 MILLIVOLTS PER DIVISION
HORIZONTAL: ONE WORD TIME

FIGURE 4-17 TYPICAL SIGNALS (Cont.)

4.8 DISPLAY UNIT TEST PROCEDURE

The procedure for testing the visual display unit is explained in the following sections.

4.8.1 Test Parameters and Tolerances

1. The voltage supplied at the junction of the four 27 K, 2 watt resistors must be +300v DC ±20%, with input voltage at 117v AC.

2. The cathode ray tube (C. R. T.) display must be sharp enough for easy identification of all bits in all registers and provide ample brightness with proper blanking.

3. All front panel adjustments must provide ample margin beyond nominal settings.

4.8.2 Calibration Test and Procedure

1. After approving all cable connections from the LGP-21 to the display unit, determine that the voltage at the junction of the four 27 K, 2 watt resistors, located at the bottom of the low voltage power supply (TB2), is +300v DC ±20% using the V. O. M. (Do not attempt to check the 1600v DC power supply. Any irregularities will inhibit scope brightness or cause multiple traces on any of the three registers.)

2. Adjust intensity, focus, and astigmatism to produce a bright, sharp trace. Clockwise rotation of the intensity control must increase brightness.

3. Adjust the position controls for the C, R and A register to obtain a trace in each of the proper locations. Clockwise rotation of each control must move only one trace downward. Carefully rotate the C. R. T. by its exposed connector so that all traces are perfectly horizontal.

4. Load a pattern of F's into the accumulator from the Flexowriter, fill into the instruction register, and execute this "U" command to load the counter. Adjust bit size for comfortable viewing. Clockwise rotation increases bit size.

5. Adjust the variable ceramic capacitor (275-970 ufd.), located on the low voltage power supply, to produce a perfect square wave for each bit without any distortion.

6. Adjust horizontal gain and centering controls for an approximately correct display.

   Clockwise rotation of the H Gain control must lengthen all traces.

   Clockwise rotation of the centering control must move all traces to the right.

   Perform steps 2, 3, and 4 again if needed.

7. Fine Horizontal Adjustment:

   a. Adjust the centering control so that the least significant or furthest right bit is properly positioned to the scope mask.

   b. Adjust the horizontal gain control so that the most significant or furthest left bit is properly positioned to the scope mask.

   c. Adjust the horizontal linearity potentiometer (the only Trimpot mounted on the printed circuit card) so that the center bits are properly positioned to the scope mask.

      NOTE: All three controls interact, so it will be necessary to repeat operations a, b, and c in sequence until a perfect trace is presented.

8. Adjust intensity so that only the track, sector, and overflow bits are displayed in the counter. All other bits must be blanked, although they will be displayed faintly if the brightness is high.

9. None of the front panel controls should require a setting of more than approximately 25% from the minimum or maximum to provide a sharp accurate display.

Section 5

Logic Diagrams

SECTION V

LOGIC DIAGRAMS

PREFACE

Logic diagrams of the Memory Control Board, Phase Control Board, P and Q Register Board, Arithmetic, Flex-Tally I/O Board, and Tally P and R Board are included as an aid in trouble-shooting. The interconnection between the Flexowriter and Computer and the Tally Reader and Computer can be found in the cabling diagrams, Section VI.

KCRI is picked by Sr which allows KRC to pick.

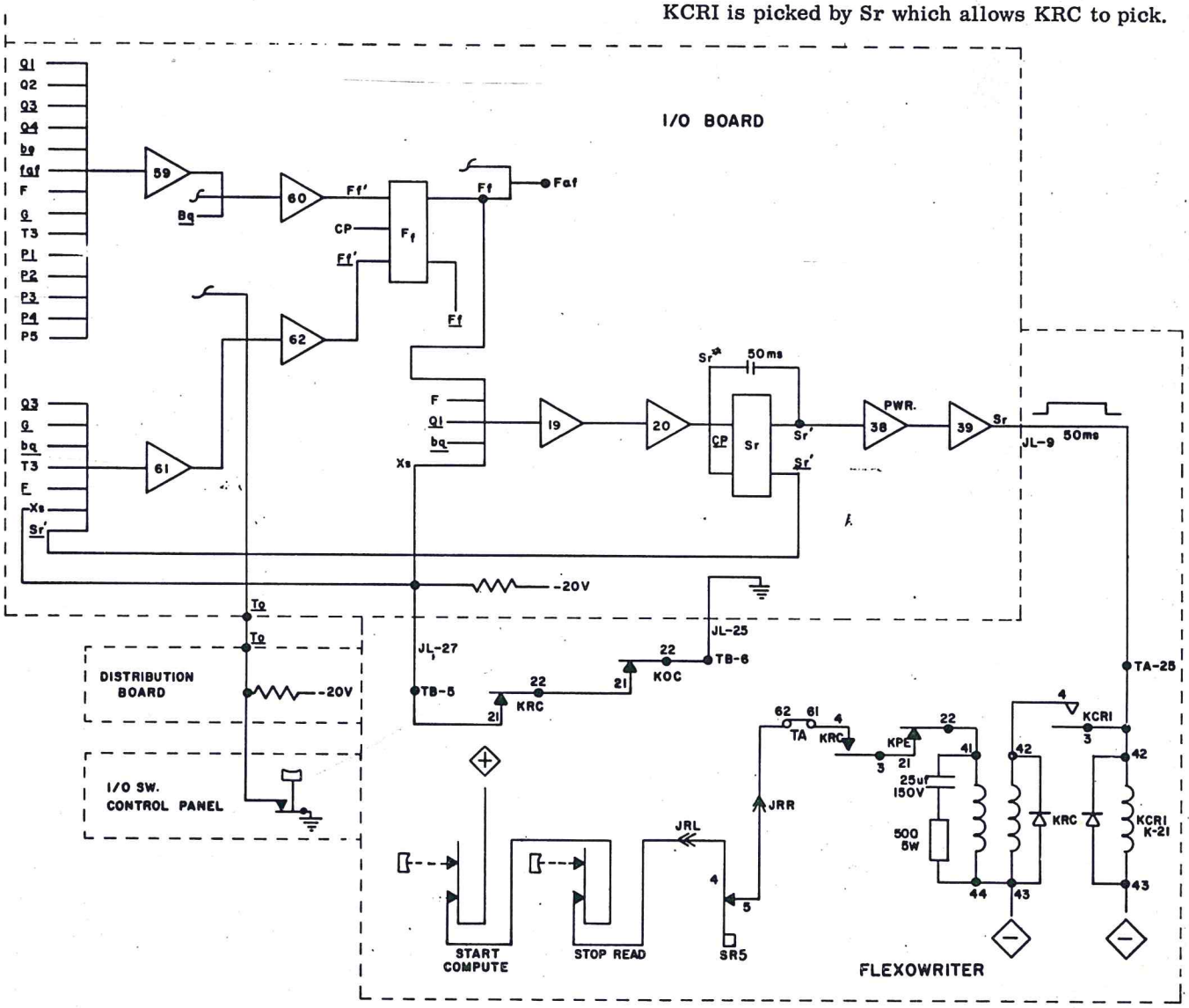


FIGURE 5-1(a) FLEXOWRITER FUNCTIONS DURING THE EXECUTION OF AN INPUT ORDER

After 50 ms KCRI drops out and provides a pick path for KOC as shown below:

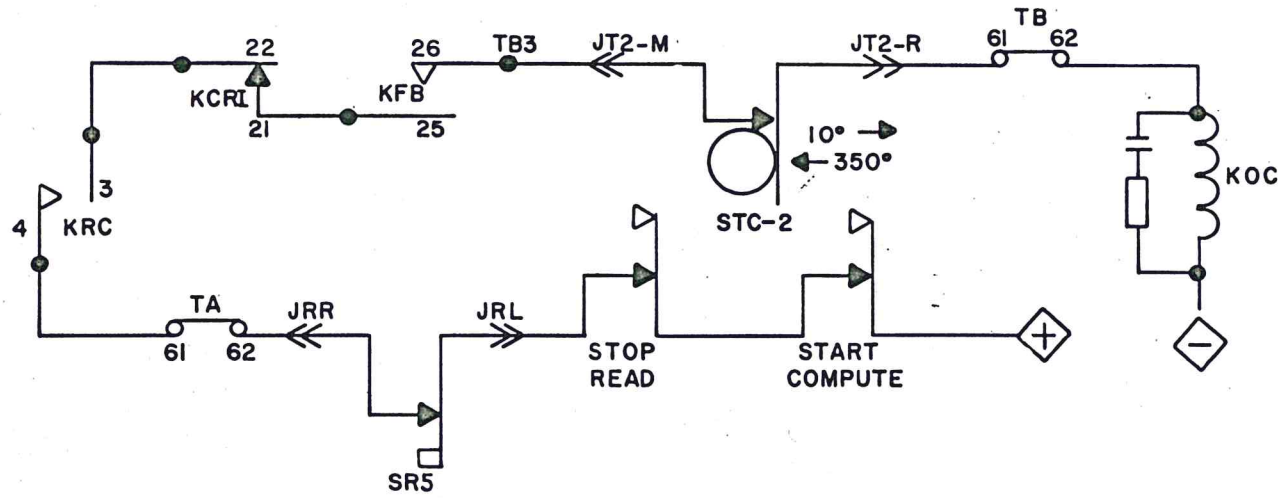


FIGURE 5-1(b) FLEXOWRITER FUNCTIONS DURING THE EXECUTION OF AN INPUT ORDER (Cont.)

When KOC picks, the reader clutch may be picked, dependent on the position of the manual input button.

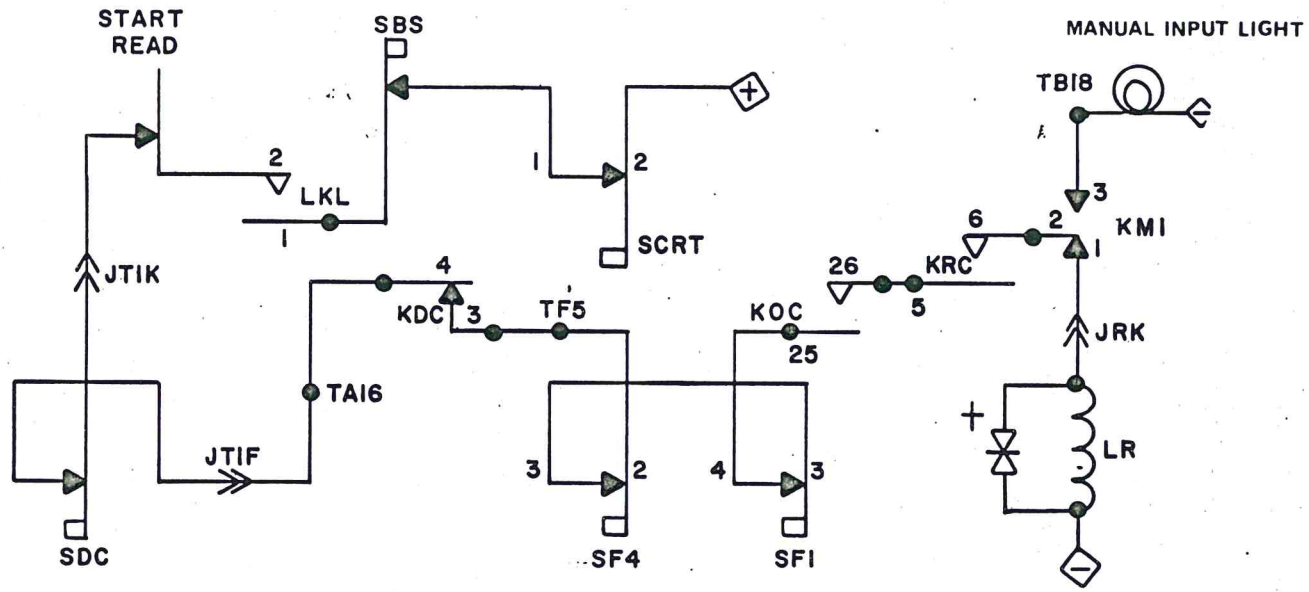


FIGURE 5-1(c) FLEXOWRITER FUNCTIONS DURING THE EXECUTION OF AN INPUT ORDER (Cont.)

If the manual input button is not depressed, KMI is not picked and the reader will advance the tape. At this time the computer is in phase one. When the combination of SC6 through SC12 contacts are made, which correspond to the character read from the tape, SC7 makes placing -20v on JL-12 which becomes the term Fc and forces phase 3. At the same time -20v is available on the transferred SC contacts to set the P flip-flops. Phase three continues until SC7 restores, placing -20v on JL-11. This becomes the signal Gc which will cause the computer to enter phase four.

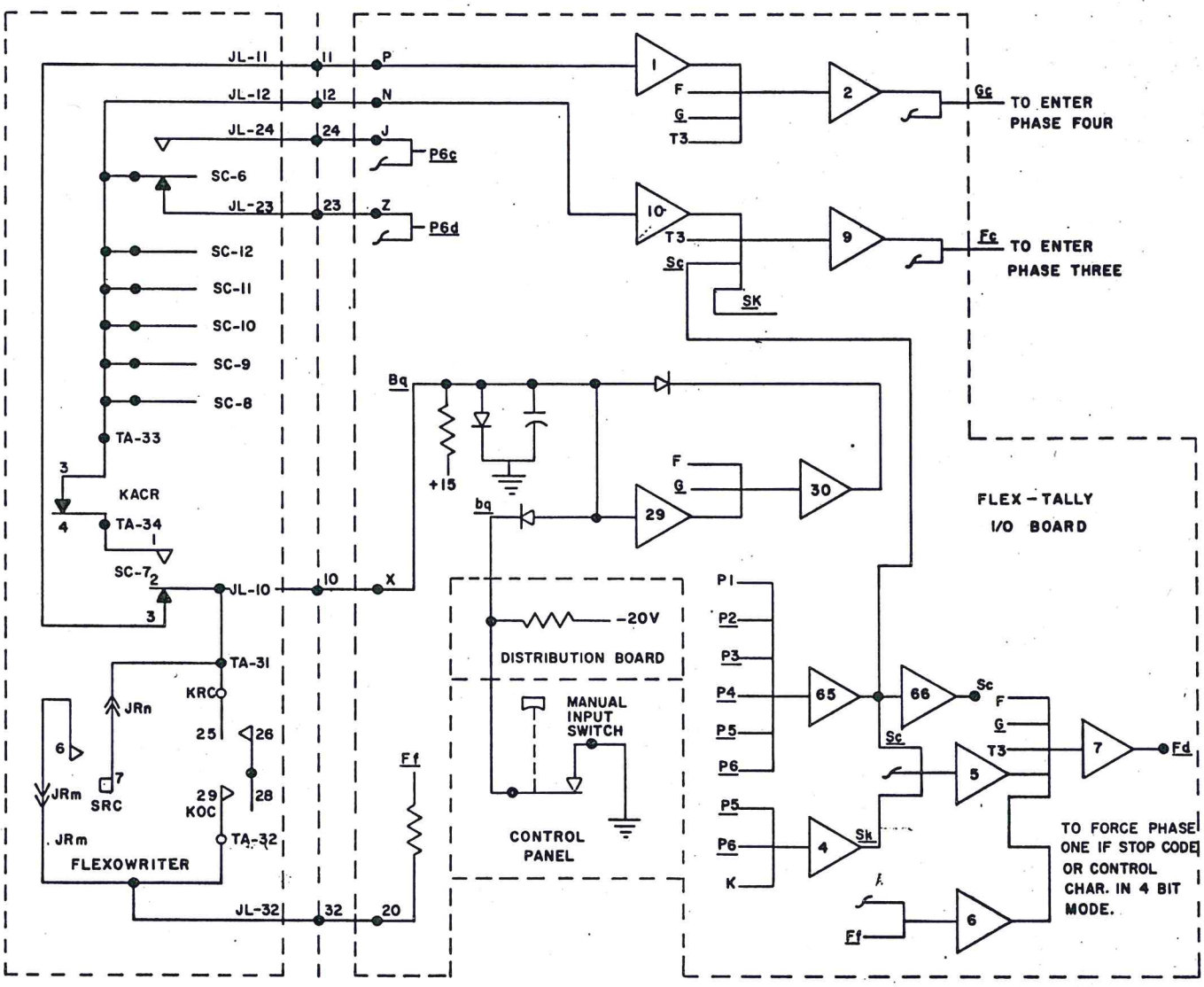


FIGURE 5-1 (d) FLEXOWRITER FUNCTIONS DURING THE EXECUTION OF AN INPUT ORDER (Cont.)

Assuming the flexowriter translator to be latched, at sign time of the first phase one after Ff and the output indicator (Q3) have been turned on, the term "X" will come true for one bit-time. This will provide gating to set both the translator storage drivers and the translator clutch storage driver. The translator magnets and clutch are picked simultaneously. At 20° of the translator rotation, the -48v supply is removed from the common side of the translator magnets and is not restored until 320°. At 250°, STC-4 contacts break, placing -20v on JL-33 to prevent "X" from being turned on during the resetting of the translator storage drivers. STC-3 contacts place -20v on JL-29 between 260° and 300°. This will reset the translator clutch and magnet drivers. At 310°, "X" is again allowed to come true to set the storage drivers, which in turn will pick the translator magnets and clutch as soon as STC-1 contacts make at 320°.

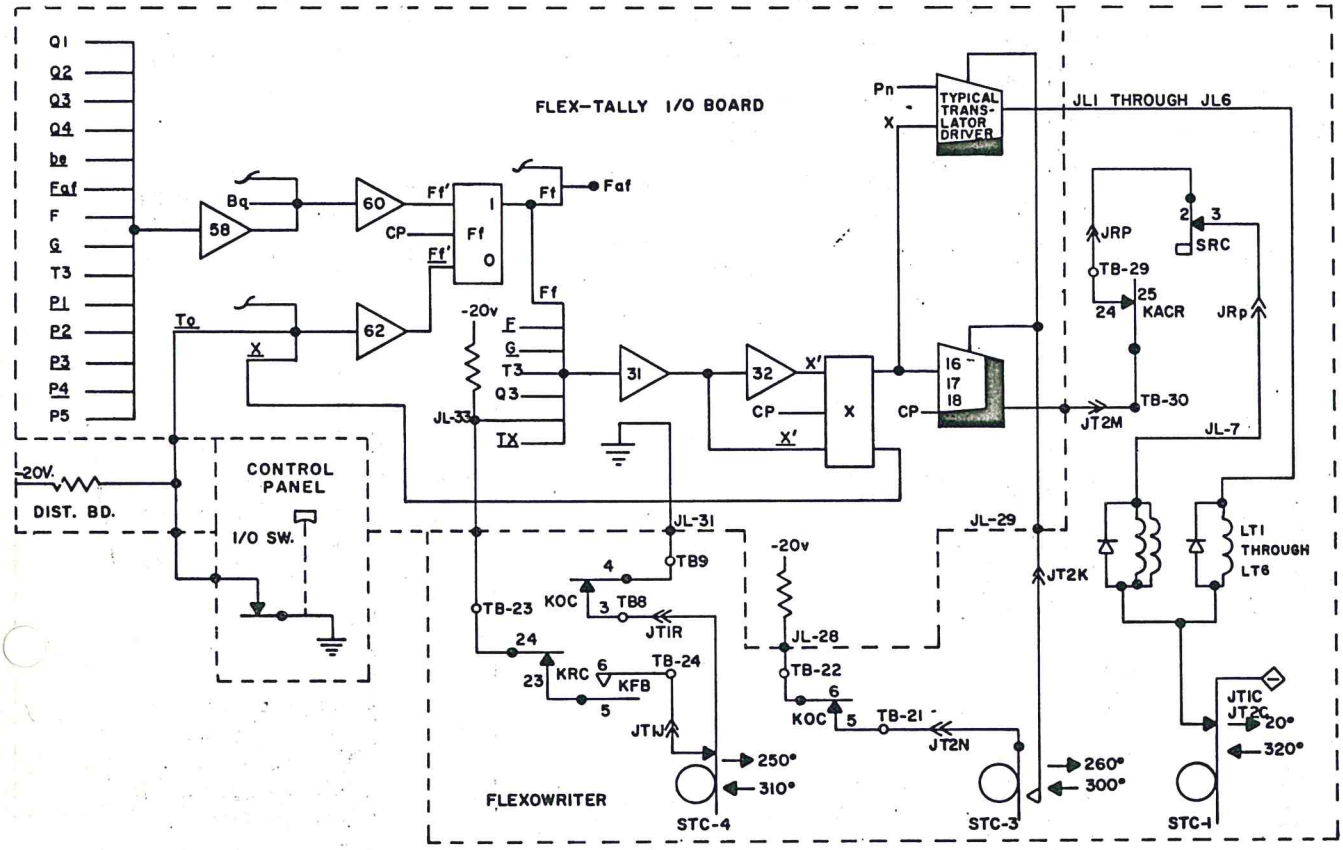


FIGURE 5-2 PRINT (ON THE FLEXOWRITER)

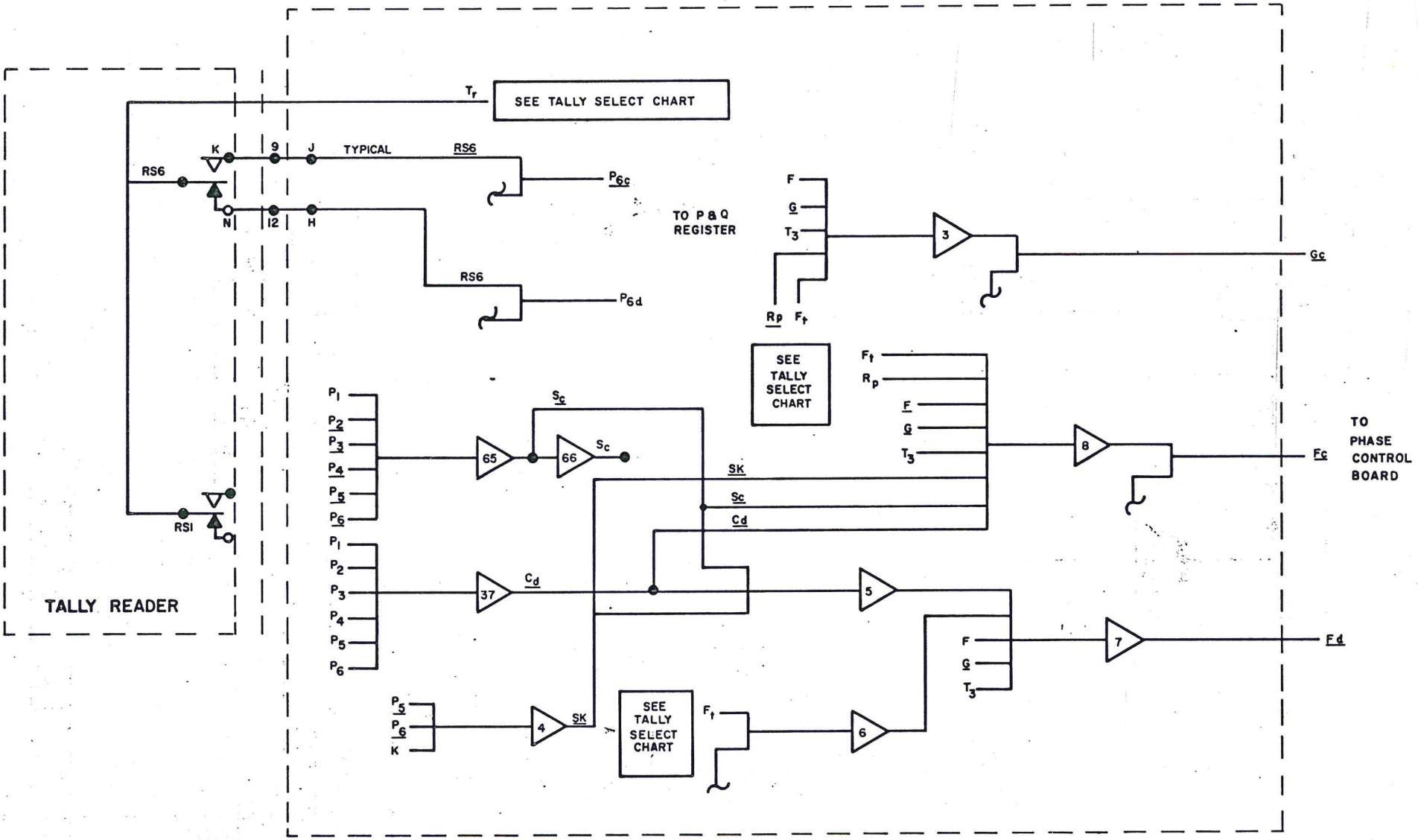


FIGURE 5-3 TALLY READER INPUT

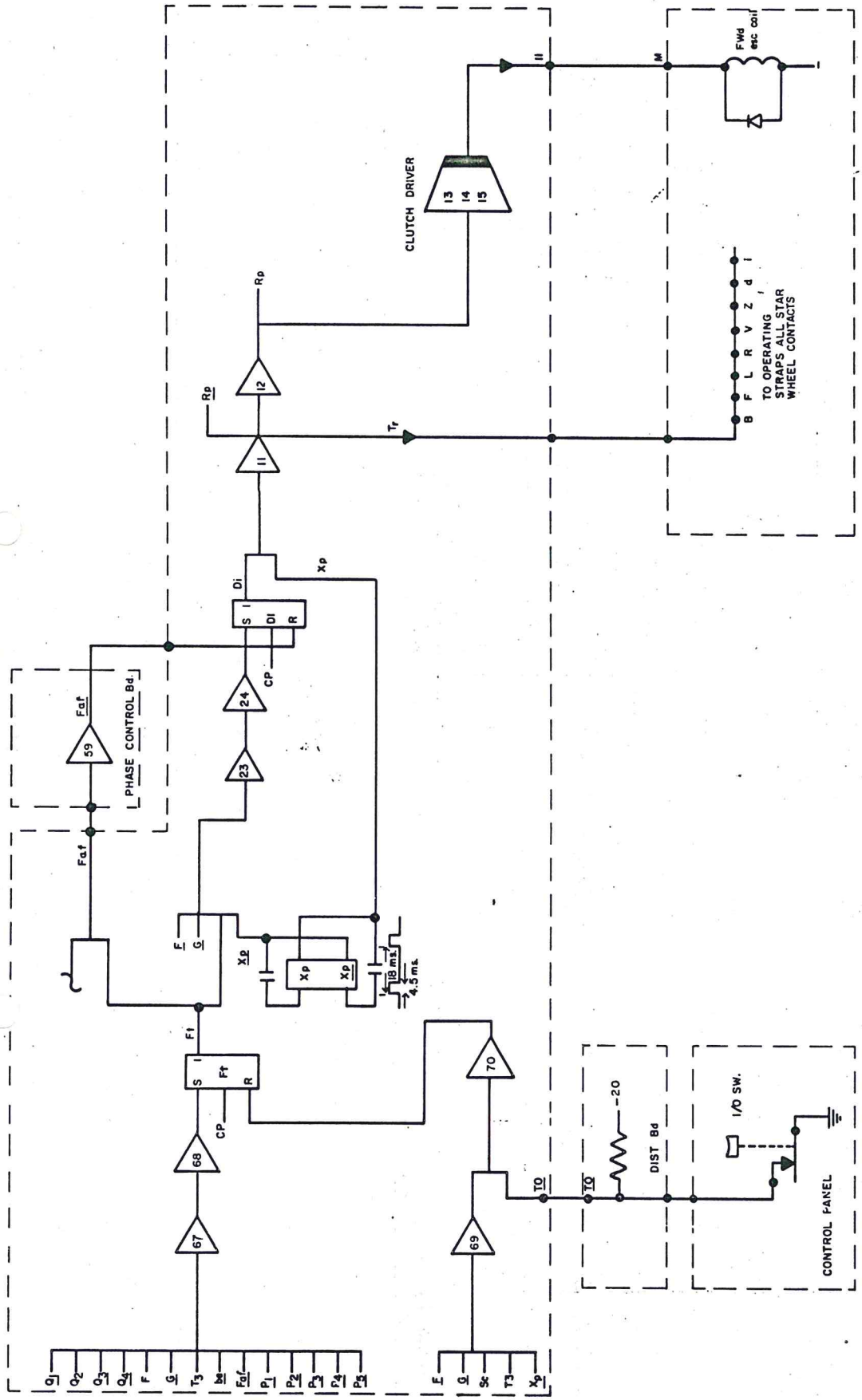
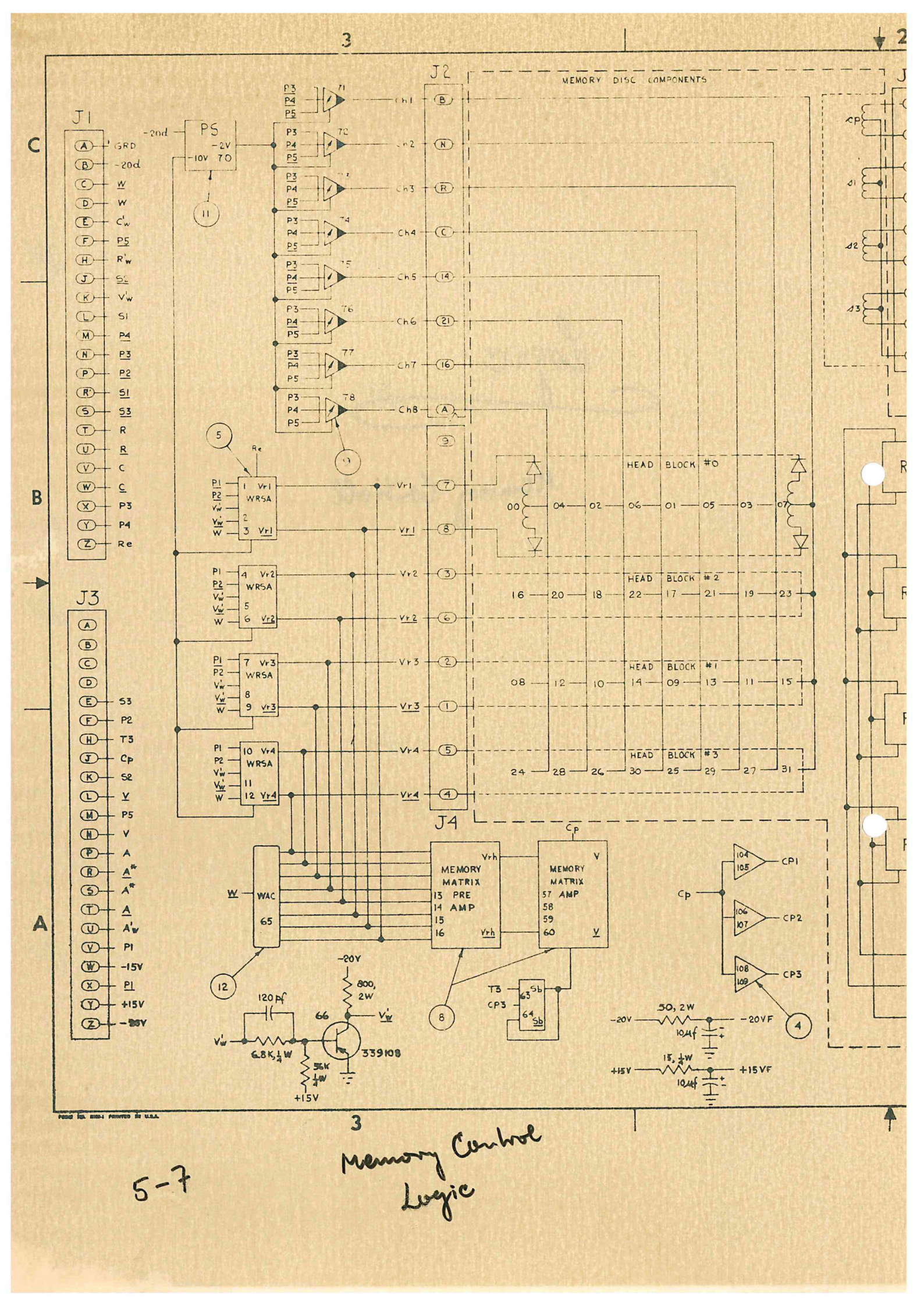


FIGURE 5-4 TALLY READER SELECT

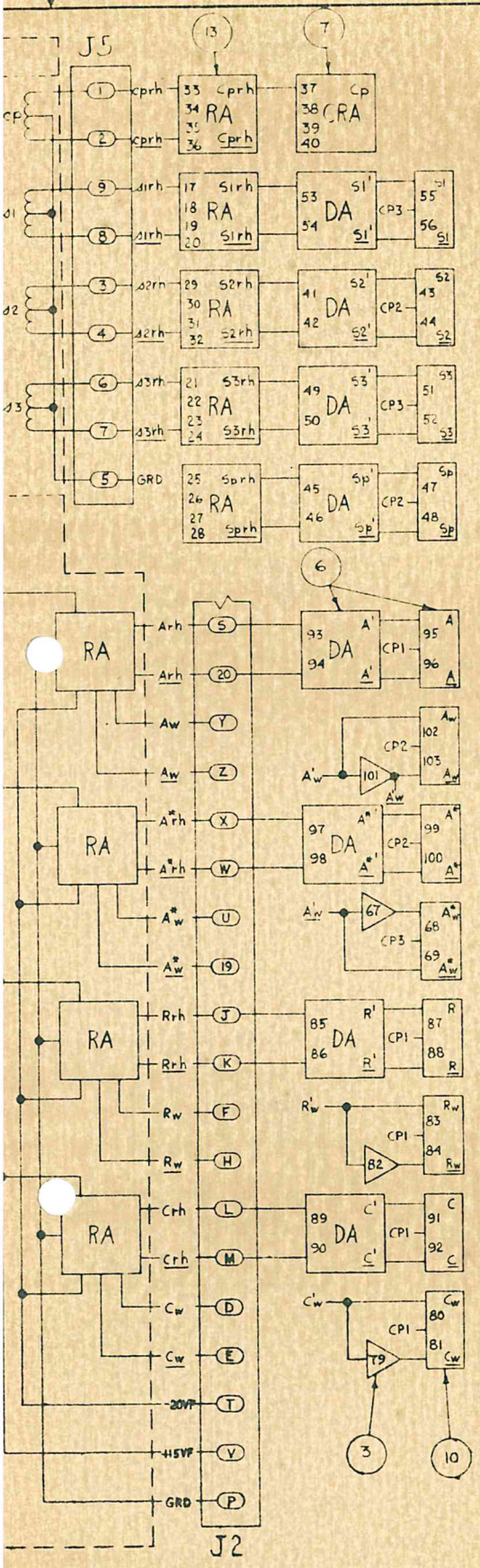
Logic

Memory Control



5-7

Memory Control Logic



REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED
O		RELEASE TO PRODUCTION	8-22-62	
1		REVISED PER LTR 101960	8-22-62	

ITEM NO.	QTY REQD	PART OR IDENTIFYING NO.	MATERIAL SIZE, DESCRIPTION & SPECIFICATION
13	5	(L543) 339598	READ AMPLIFIER
12	1	(L543) 338449	WRITE AMPLIFIER CLAMP
11	1	(L543) 338448	-10V & -2V POWER SUPPLY
10	5	(L543) 338447	RECIRCULATING REGISTER WRITE AMPLIFIER
9	8	(L543) 338446	CHANNEL SELECTOR
8	1	(L543) 338445	MATRIX READ AMPLIFIER
7	1	(L543) 338444	CLOCK READ AMPLIFIER
6	8	(L543) 338442	DATA AMPLIFIER
5	4	(L543) 338441	WRITE & READ SELECTION AMPLIFIER
4	3	(L543) 338434	CLOCK DRIVER
3	4	(L543) 338428	NOR GATE
2	1	L535 004654	ASSEMBLY
1	1	L535 004653	CIRCUIT BOARD

SCHEMATIC

SCHEMATIC

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DIMENSIONS
DECIMAL — ANGULAR
2 PLACE ± 02 — ± 1°
3 PLACE ± 010
4 PLACE ± 0005
MATERIAL
FINISH

DRAWING GRADE
DR 13 APR 62
CHK
ENGR 23 APR 62
APPD 24 APR 62
ISSUED BY

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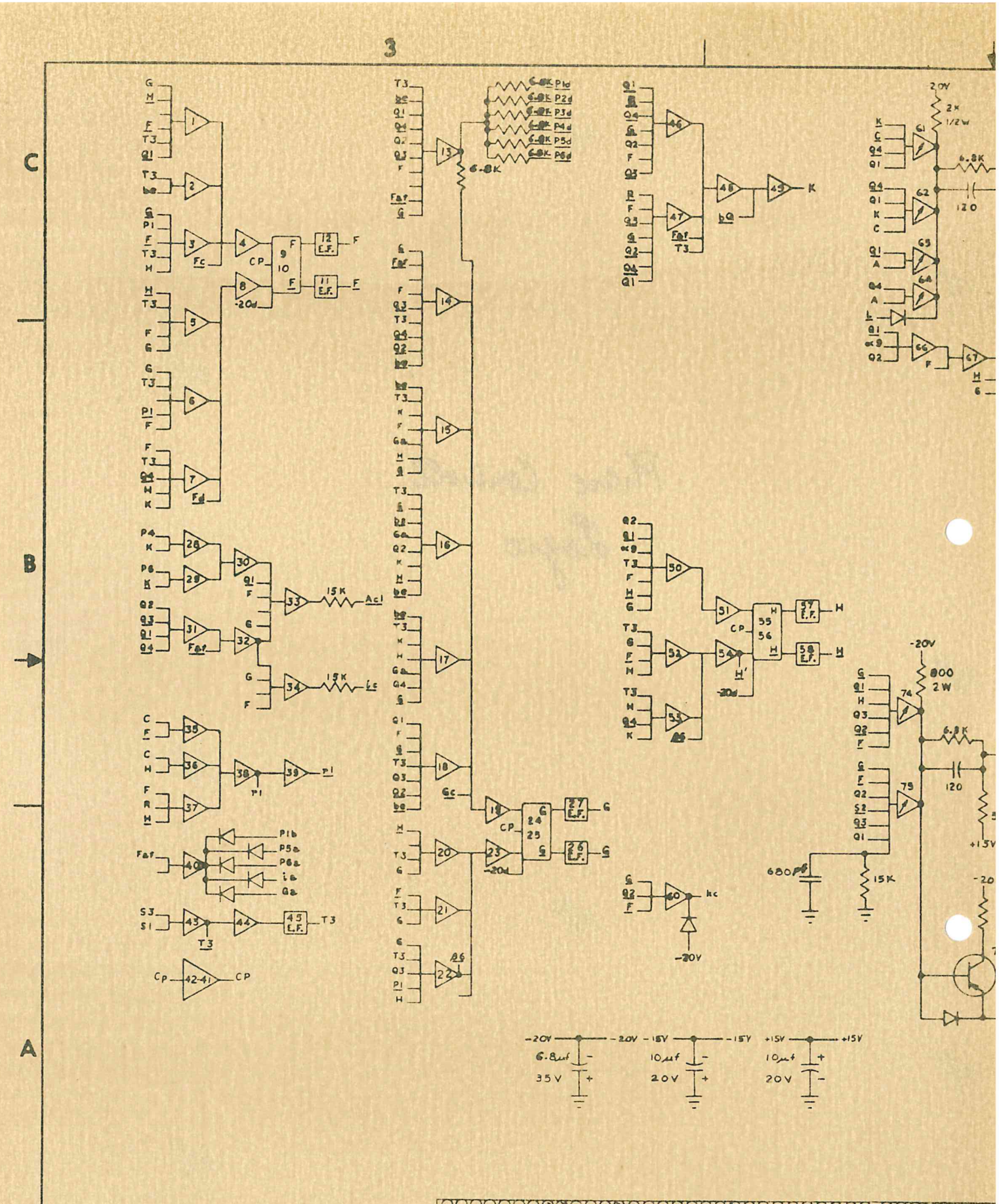
MEMORY CONTROL
L12I COMPUTER
LOGIC DIAGRAM

CODE IDENT NO. 36090 | SIZE D | L200 011 842
SCALE | SHEET

L200011842

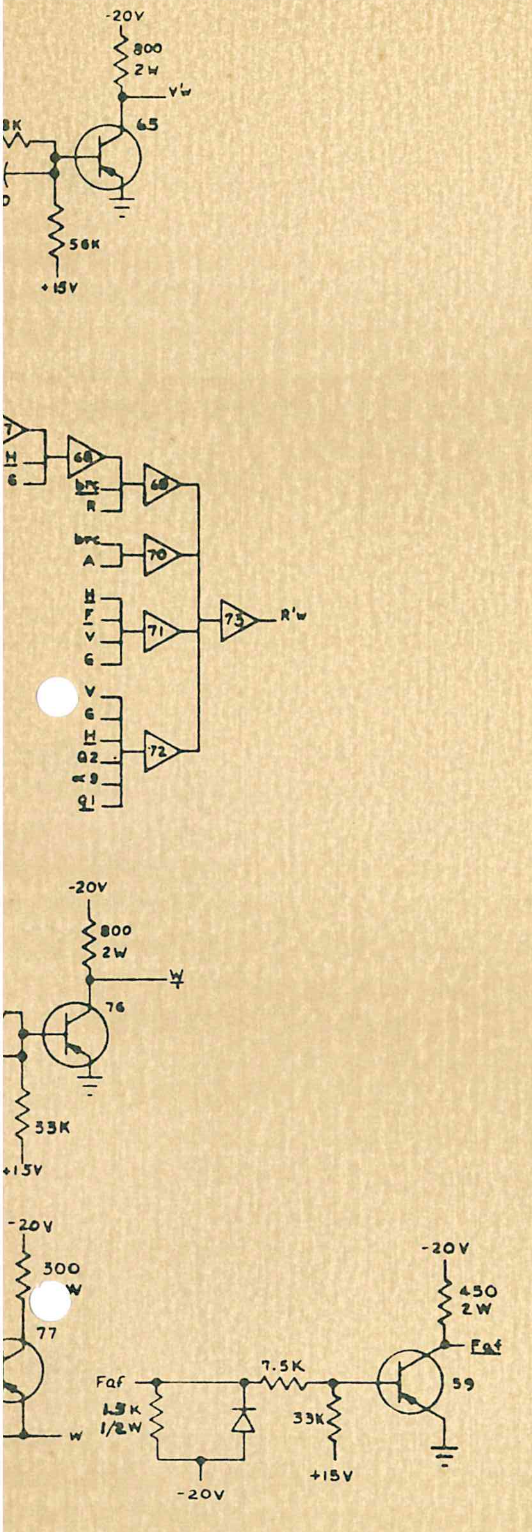
Phase Control

Logic



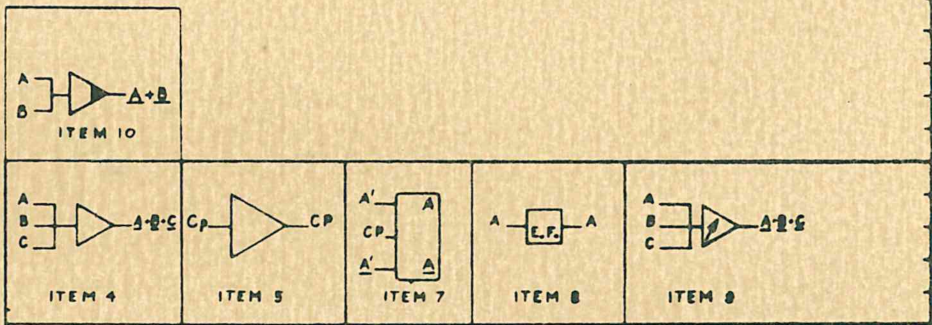
5-8

Phase Control Logic



REVISIONS

SYM	ZONE	DESCRIPTION	DATE	APPROVED
0		RELEASE TO PRODUCTION.		
1		REVISED PER E.O. 97307		
2		REVISED PER E.O. 101969		
3		REVISED PER E.O. 101989		
4		REVISED PER E.O. 105140		



ITEM NO.	QTY REQD	PART OR IDENTIFYING NO.	MATERIAL SIZE, DESCRIPTION & SPECIFICATION
10	2	(L543) 338429	LOW Zo NOR GATE
9	6	(L543) 338430	DIODE COUPLED GATE SCHEMATIC
8	7	(L543) 338433	EMITTER FOLLOWER
7	3	(L543) 338431	FLIP FLOP
6	3	TRANSISTOR 65,76,77	SPECIAL CIRCUIT
5	1	(L543) 338434	CLOCK DRIVER
4	51	(L543) 338428	NOR GATE SCHEMATIC
3	1	(L535) 339562	ASSEMBLY
2	1	(L535) 339561	CIRCUIT BOARD
1	1	(L535) 339561	MASTER LAYOUT

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DIMENSIONS
DECIMAL: 2 PLACE ±.02, 3 PLACE ±.010, 4 PLACE ±.0005
ANGULAR: ±1°
MATERIAL
FINISH

DRAWING GRADE
DR
CHK
ENGR
APPD
ISSUED BY

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LIBRASCOPE DIVISION · GENERAL PRECISION, INC. GLENDALE 1, CALIFORNIA

LOGIC DIAGRAM
PHASE CONTROL
LGP-21 COMPUTER

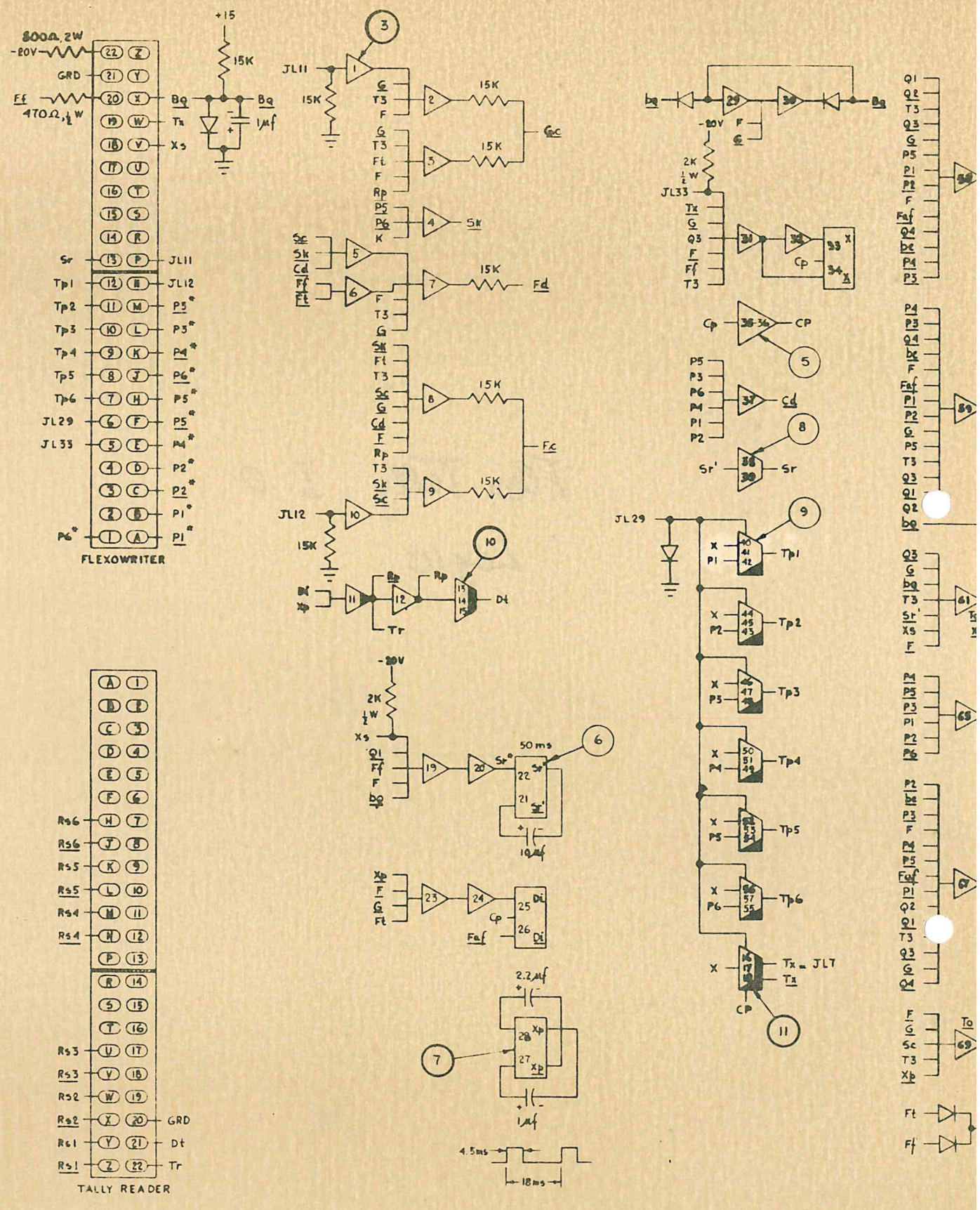
CODE IDENT NO.	SIZE	
36090	D	339559
SCALE		SHEET

(L200)

FIGURE 5-6 PHASE CONTROL LOGIC DIAGRAM

Flex Tally I O

Logic



2. REFERENCE CIRCUIT BOARD ASSEMBLY (L535) 339566
1. UNLESS OTHERWISE NOTED, DIODES ARE 339178

NOTES:

FORM NO. 5351 PRINTED IN U.S.A.

5-11

Flex to Tally Logic

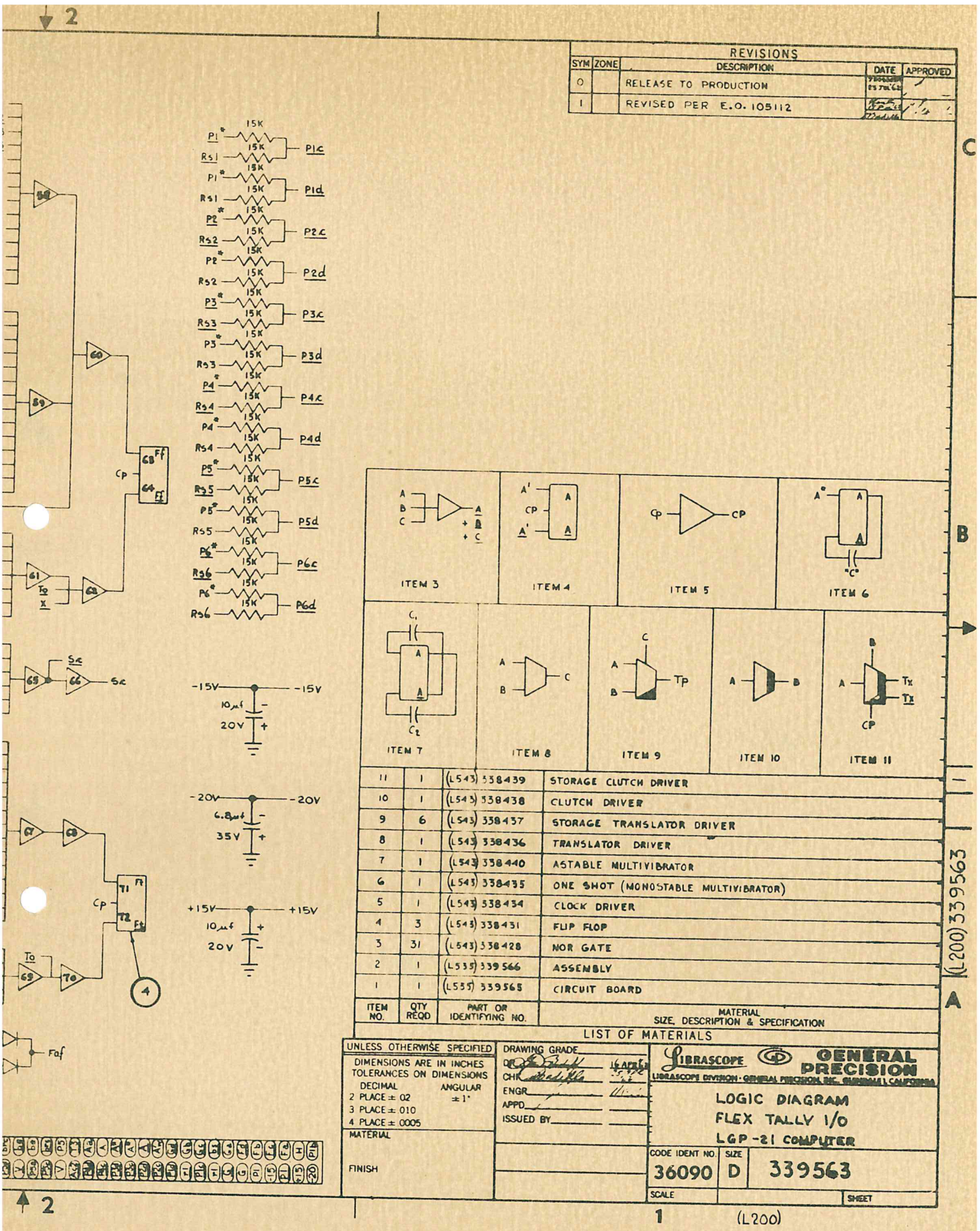
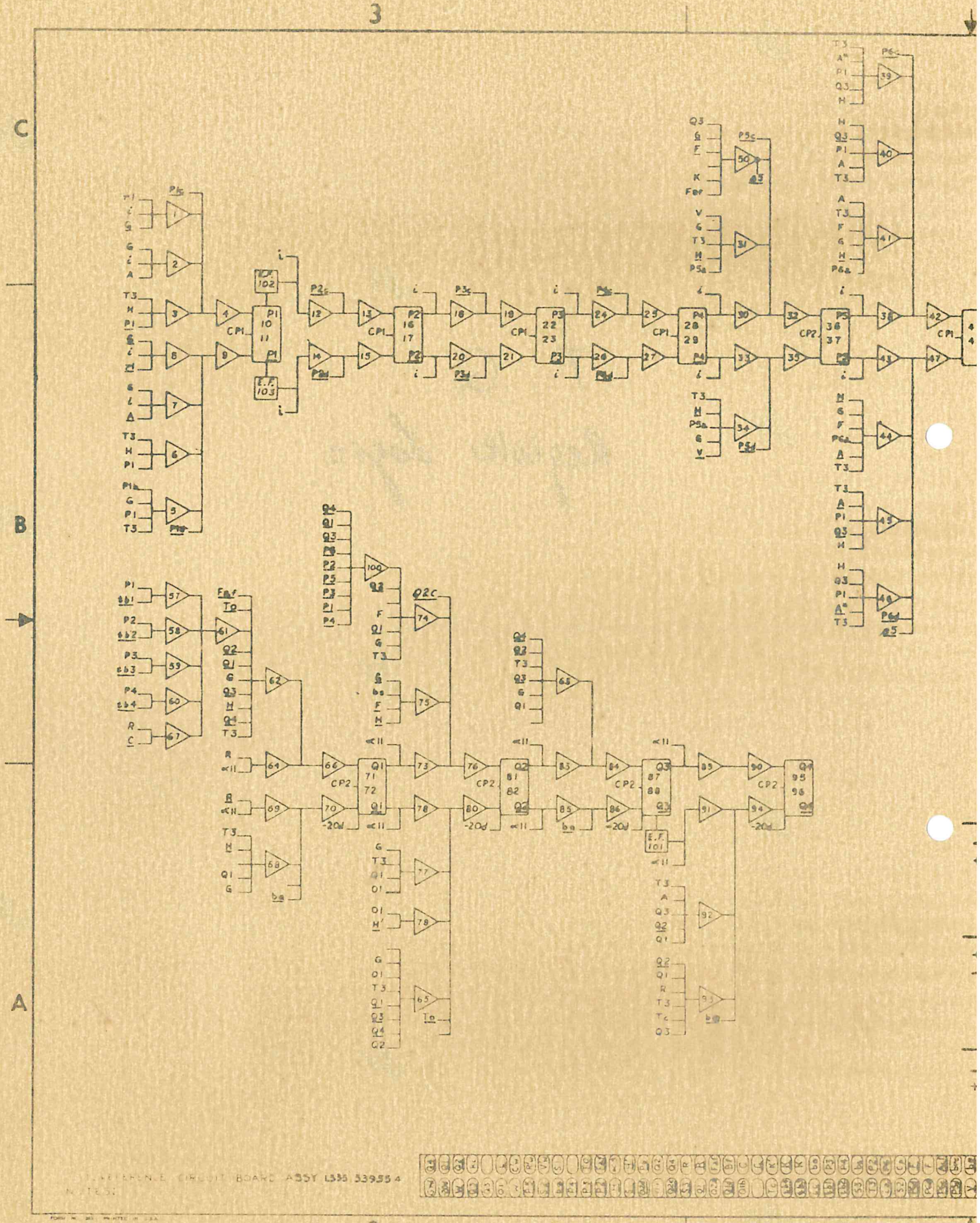


FIGURE 5-9 FLEX-TALLY I/O LOGIC DIAGRAM

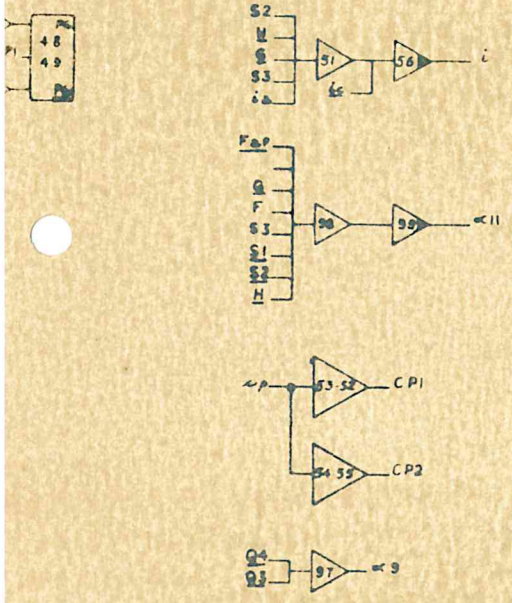
P Q

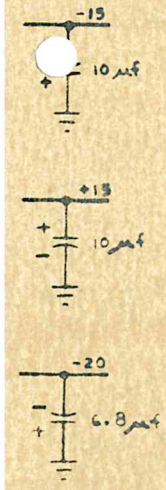
Register Logic

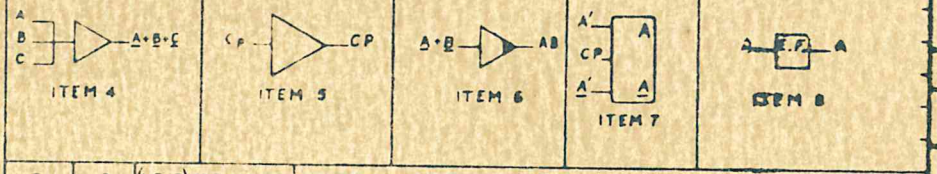

3
C
B
A
CP1
CP2
P1
P2
P3
P4
E.F. 102
E.F. 103
E.F. 101
Q2C
-20d
P + R Register
Logic

5-9

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED
0		RELEASE FOR PRODUCTION		
1		REVISED PER E.O. 101971		
2		REVISED PER E.O. 101995		
3		REVISED PER E.O. 102081		
4		REVISED PER E.O. 109913		







ITEM NO	QTY REQD	PART OR IDENTIFYING NO	MATERIAL SIZE, DESCRIPTION & SPECIFICATION
8	3	(L543) 338433	EMITTER-FOLLOWER SCHEMATIC
7	10	(L543) 338431	FLIP FLOP
6	2	(L543) 338429	NOR GATE, LOW Z0
5	2	(L545) 338434	CLOCK DRIVER
4	74	(L543) 338428	NOR GATE SCHEMATIC
3	1	(L535) 339554	ASSEMBLY (REF)
2	1	(L535) 339551	CIRCUIT BOARD (REF)
1	1	(L535) 339553	MASTER LAYOUT (REF)

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DIMENSIONS
DECIMAL ANGULAR
2 PLACE ± 02 ±1°
3 PLACE ± 010
4 PLACE ± 0005
MATERIAL
FINISH

DRAWING GRADE
DR
CHK
MGR
APPD
ISSUED BY

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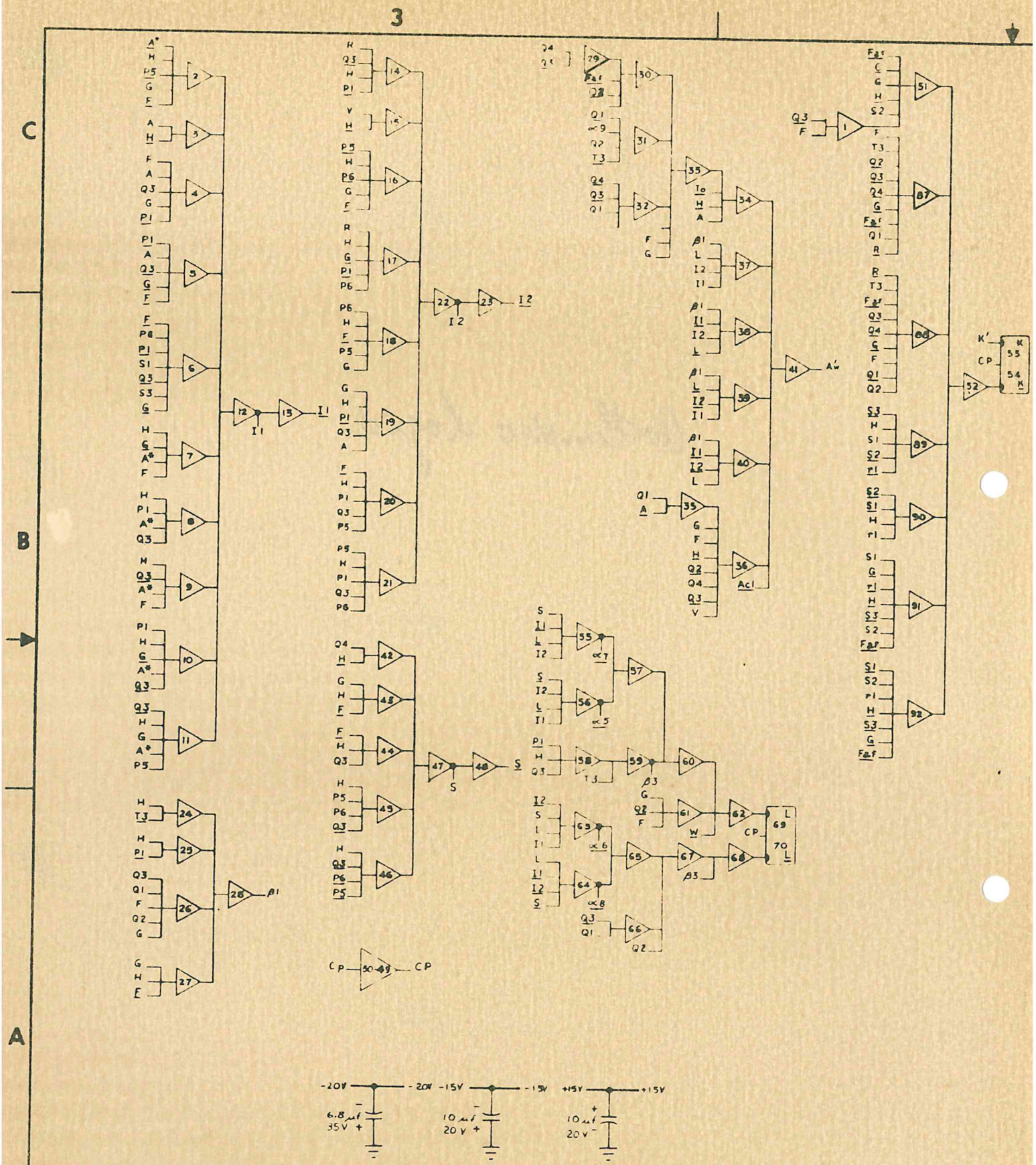
LOGIC DIAGRAM P&Q REGISTER LGP-21 COMPUTER

CODE IDENT NO	SIZE	
36090	D	339551
SCALE		SHEET

(L200) 339551

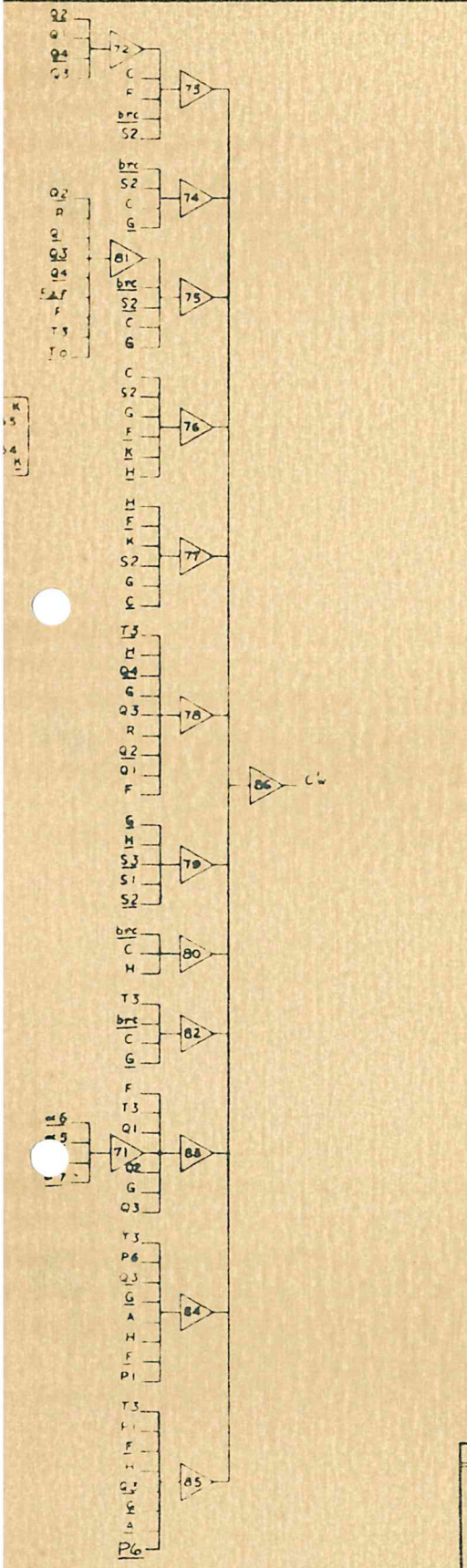
FIGURE 5-7 P AND Q REGISTER LOGIC DIAGRAM

Arithmetic Logic



NOTES: 1. REFERENCE BOARD ASSEMBLY (L535)339558

FIGURE 5-8 ARITHMETIC LOGIC DIAGRAM



ITEM 4

ITEM 5

ITEM 6

ITEM NO	QTY REQD	PART OR IDENTIFYING NO	MATERIAL SIZE, DESCRIPTION & SPECIFICATION
6	2	(L543) 338432	LOW Z FLIP FLOP SCHEMATIC
5	1	(L543) 338434	CLOCK DRIVER SCHEMATIC
4	85	(L543) 338428	NOR GATE SCHEMATIC
3	1	(L535) 339558	ASSEMBLY
2	1	(L535) 339557	CIRCUIT BOARD
1	1	(L535) 339557	MASTER LAYOUT

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DIMENSIONS
DECIMAL ANGULAR
2 PLACE ± 02 ±1°
3 PLACE ± 010
4 PLACE ± 0005
MATERIAL
FINISH

DRAWING GRADE
DR J.R. Fernandez 22 MAR 62
CHK W Gabello 12 MAR 62
ENGR L. Bailey 7/6/62
APPD
ISSUED BY

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LIBRASCOPE DIVISION · GENERAL PRECISION, INC., GLENDALE 1, CALIFORNIA

LOGIC DIAGRAM
ARITHMETIC
LGP-21 COMPUTER

CODE IDENT NO	SIZE	
36090	D	339555
SCALE		SHEET

(L200)

.200 339 555 | 2 | A

Revised March, 1964

5-10

Section 6

Schematics

SIGNAL	CARD	PAGE	LOC.	SIGNAL	CARD	PAGE	LOC.	SIGNAL	CARD	PAGE	LOC.
Acl	Phase Control	6-9	B-2	F	Phase Control	6-9	C-2	Q1	P & Q Register	6-23	C-2
Aw'	Arithmetic	6-27	B-2	Faf	Phase Control	6-9	B-1	Q1	P & Q Register	6-23	C-2
Arh	Memory Control Bd.	6-7	C-3	Fc	Flex-Tally I/O	6-13	C-3	Q2	P & Q Register	6-23	C-1
Arh	Memory Control Bd.	6-7	C-3	Fd	Flex-Tally I/O	6-13	B-2	Q2	P & Q Register	6-23	C-1
Aw'	Memory Control Bd.	6-7	A-3	Ff	Flex-Tally I/O	6-15	C-1	Q3	P & Q Register	6-23	B-2
Aw'	Memory Control Bd.	6-7	A-3	Ff	Flex-Tally I/O	6-15	C-1	Q3	P & Q Register	6-23	A-1
Aw	Memory Control Bd.	6-7	B-3	Ft	Flex-Tally I/O	6-15	A-1	Q4	P & Q Register	6-25	C-2
Aw	Memory Control Bd.	6-7	B-3	Ft	Flex-Tally I/O	6-15	B-1	Q4	P & Q Register	6-25	C-2
A*rh	Memory Control Bd.	6-7	C-3	Faf	Flex-Tally I/O	6-15	A-1	rl	Phase Control	6-9	B-1
A*rh	Memory Control Bd.	6-7	C-3	G	Phase Control	6-11	B-2	rl	Phase Control	6-9	C-1
A*	Memory Control Bd.	6-7	C-2	G	Phase Control	6-11	C-2	Rw'	Phase Control	6-11	C-1
A*	Memory Control Bd.	6-7	C-2	Gc	Flex-Tally I/O	6-13	B-3	Rp	Flex-Tally I/O	6-13	B-2
Aw*	Memory Control Bd.	6-7	B-2	H	Phase Control	6-9	B-1	Rp	Flex-Tally I/O	6-13	B-2
Aw*	Memory Control Bd.	6-7	B-2	H	Phase Control	6-9	B-1	Rrh	Memory Control Bd.	6-7	C-2
9	P & Q Register Bd.	6-17	A-2	HB#0	Memory Control	6-3	C-2	Rrh	Memory Control Bd.	6-7	C-2
11	P & Q Register Bd.	6-17	A-3	HB#1	Memory Control	6-3	B-2	R	Memory Control Bd.	6-7	C-1
7	Arithmetic	6-27	C-2	HB#2	Memory Control	6-3	B-2	R	Memory Control Bd.	6-7	C-1
8	Arithmetic	6-27	A-2	HB#3	Memory Control	6-3	A-2	Rw'	Memory Control Bd.	6-7	B-2
6	Arithmetic	6-27	B-2	ic	Phase Control	6-9	A-2	Rw	Memory Control Bd.	6-7	B-2
5	Arithmetic	6-27	C-2	i	P & Q Register	6-21	B-3	Rw	Memory Control Bd.	6-7	B-1
A	Memory Control Bd.	6-7	C-3	I1	Arithmetic	6-29	C-2	Sk	Flex-Tally I/O	6-13	A-3
A	Memory Control Bd.	6-7	C-3	I1	Arithmetic	6-29	C-2	Sr'	Flex-Tally I/O	6-13	A-1
B6	Phase Control	6-11	A-2	I2	Arithmetic	6-29	C-1	Sr'	Flex-Tally I/O	6-13	B-1
BQ	Flex-Tally I/O Bd.	6-13	B-1	I2	Arithmetic	6-29	C-1	Sr	Flex-Tally I/O	6-13	A-1
B5	P & Q Register Bd.	6-25	B-3	K'	Phase Control	6-9	C-1	Sc	Flex-Tally I/O	6-15	C-2
B1	Arithmetic	6-31	B-1	Kc	Phase Control	6-9	A-1	Sc	Flex-Tally I/O	6-15	C-2
CP	Arithmetic	6-31	A-2	K	Arithmetic	6-31	C-2	S	Arithmetic	6-31	C-1
CP	Phase Control	6-9	A-2	K	Arithmetic	6-31	C-3	S	Arithmetic	6-31	C-1
Cd	Flex-Tally I/O Bd.	6-13	B-1	L	Arithmetic	6-27	C-1	S1	Memory Control Bd.	6-5	C-1
CP	Memory Control Bd.	6-5	C-2	L	Arithmetic	6-27	C-1	S1	Memory Control Bd.	6-5	C-1
Cw'	Arithmetic	6-33	C-1	P1c	Flex-Tally I/O	6-13	C-1	S2	Memory Control Bd.	6-5	B-1
CH-1	Memory Control Bd.	6-3	C-3	P1d	Flex-Tally I/O	6-13	C-1	S2	Memory Control Bd.	6-5	B-1
CH-2	Memory Control Bd.	6-3	C-3	P2c	Flex-Tally I/O	6-13	C-1	S3	Memory Control Bd.	6-5	A-1
CH-3	Memory Control Bd.	6-3	C-3	P2d	Flex-Tally I/O	6-13	B-1	S3	Memory Control Bd.	6-5	A-1
CH-4	Memory Control Bd.	6-3	B-3	P3c	Flex-Tally I/O	6-13	B-1	T3	Phase Control	6-9	C-2
CH-5	Memory Control Bd.	6-3	B-3	P3d	Flex-Tally I/O	6-13	B-1	T3	Phase Control	6-9	C-2
CH-6	Memory Control Bd.	6-3	B-3	P4c	Flex-Tally I/O	6-13	B-1	Tr	Flex-Tally I/O	6-13	B-2
CH-7	Memory Control Bd.	6-3	A-3	P4d	Flex-Tally I/O	6-13	B-1	TP1	Flex-Tally I/O	6-15	C-3
CH-8	Memory Control Bd.	6-3	A-3	P5c	Flex-Tally I/O	6-13	B-1	TP2	Flex-Tally I/O	6-15	B-3
Cp	Memory Control Bd.	6-5	C-2	P5d	Flex-Tally I/O	6-13	B-1	TP3	Flex-Tally I/O	6-15	B-3
Cw'	Memory Control Bd.	6-7	A-1	P6c	Flex-Tally I/O	6-13	A-1	TP4	Flex-Tally I/O	6-15	A-3
Cw	Memory Control Bd.	6-7	B-1	P6d	Flex-Tally I/O	6-13	A-1	TP5	Flex-Tally I/O	6-15	A-2
Cw	Memory Control Bd.	6-7	B-1	P1	P & Q Register	6-21	B-2	TP6	Flex-Tally I/O	6-15	B-2
CP1	Memory Control Bd.	6-5	C-1	P2	P & Q Register	6-21	C-1	Tx	Flex-Tally I/O	6-15	B-2
CP2	Memory Control Bd.	6-5	B-1	P3	P & Q Register	6-21	B-1	Vw'	Phase Control	6-11	B-1
CP3	Memory Control Bd.	6-5	B-1	P4	P & Q Register	6-21	A-1	V	Memory Control	6-3	C-1
Crh	Memory Control Bd.	6-7	C-1	P5	P & Q Register	6-25	B-2	V	Memory Control	6-3	C-1
Crh	Memory Control Bd.	6-7	C-1	P6	P & Q Register	6-25	C-1	Vw'	Memory Control	6-3	A-2
C	Memory Control	6-7	C-1	P1	P & Q Register	6-21	C-2	Vw'	Memory Control	6-3	A-1
C	Memory Control	6-7	C-1	P2	P & Q Register	6-21	C-1	W	Phase Control	6-11	A-1
Di	Flex-Tally I/O	6-13	A-2	P3	P & Q Register	6-21	B-1	W	Phase Control	6-11	A-1
Di	Flex-Tally I/O	6-13	A-2	P4	P & Q Register	6-21	A-1	Xp	Flex-Tally I/O	6-13	C-2
Dt	Flex-Tally I/O	6-13	B-2	P5	P & Q Register	6-25	B-2	Xp	Flex-Tally I/O	6-13	C-2
F	Phase Control	6-9	B-2	P6	P & Q Register	6-25	C-1	X	Flex-Tally I/O	6-13	C-1
								X	Flex-Tally I/O	6-13	C-1

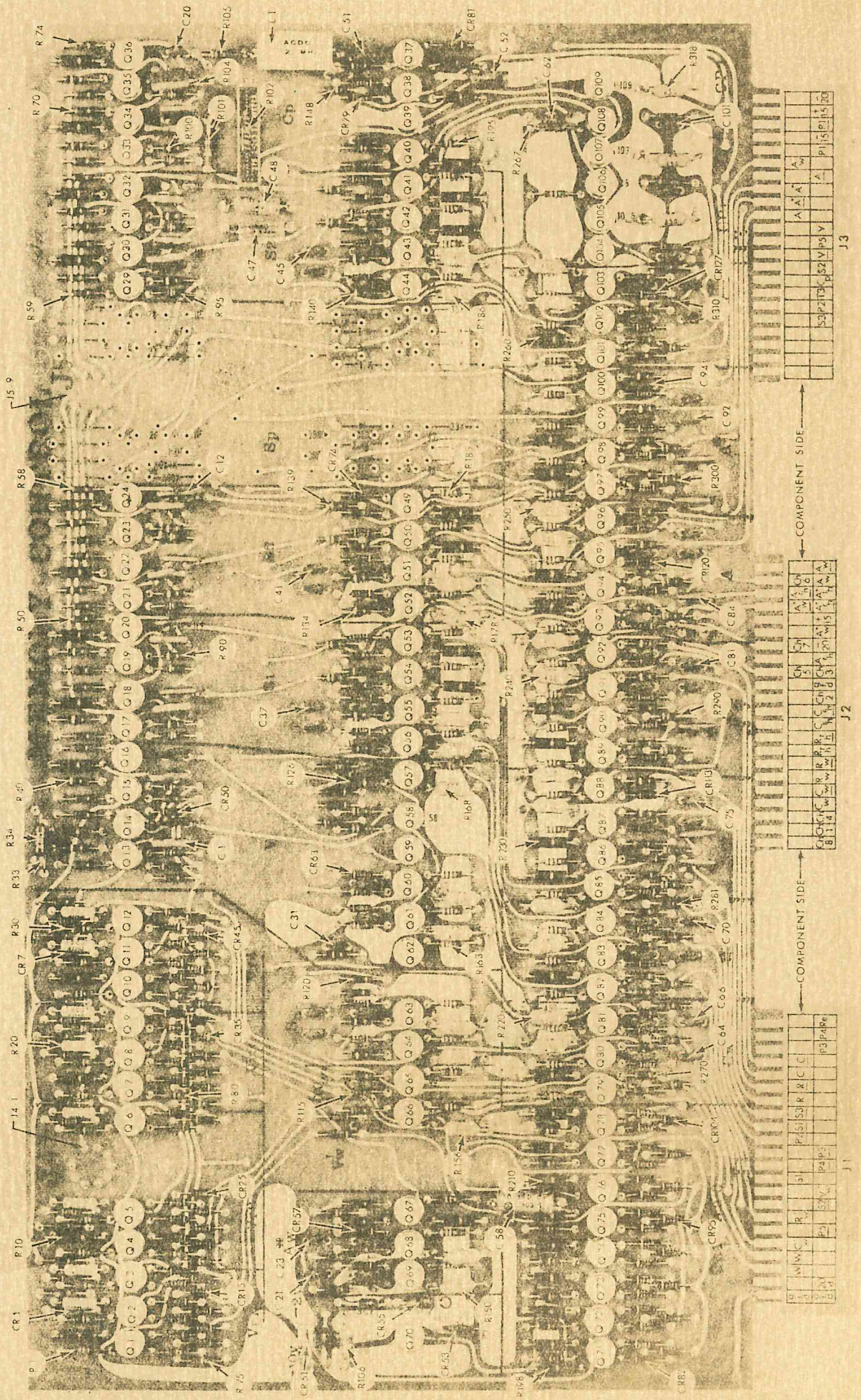
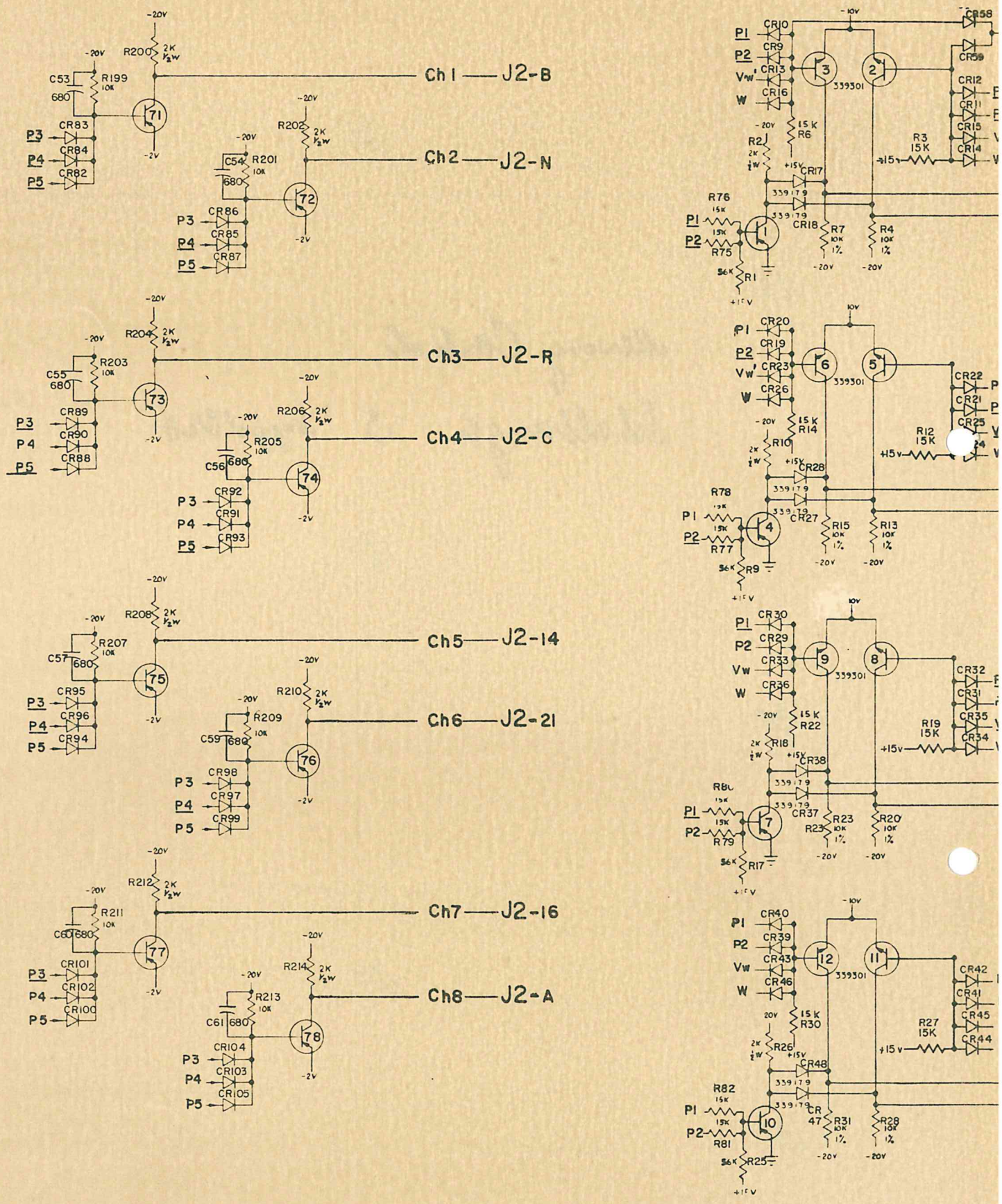


FIGURE 6-1 MEMORY CONTROL BOARD

Memory Control

Schaltungen 3 Doppelblatt

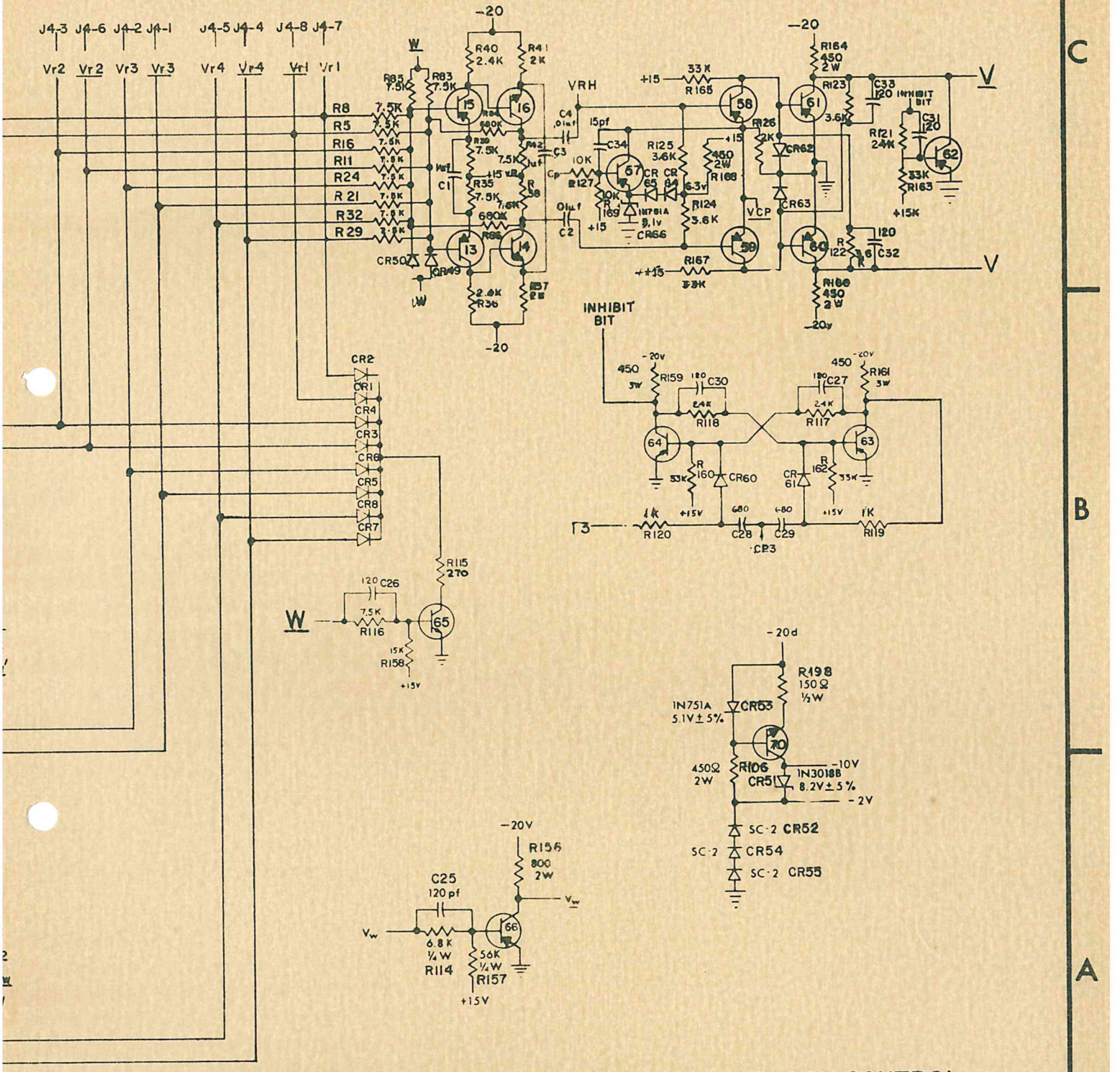


Revised March, 1964

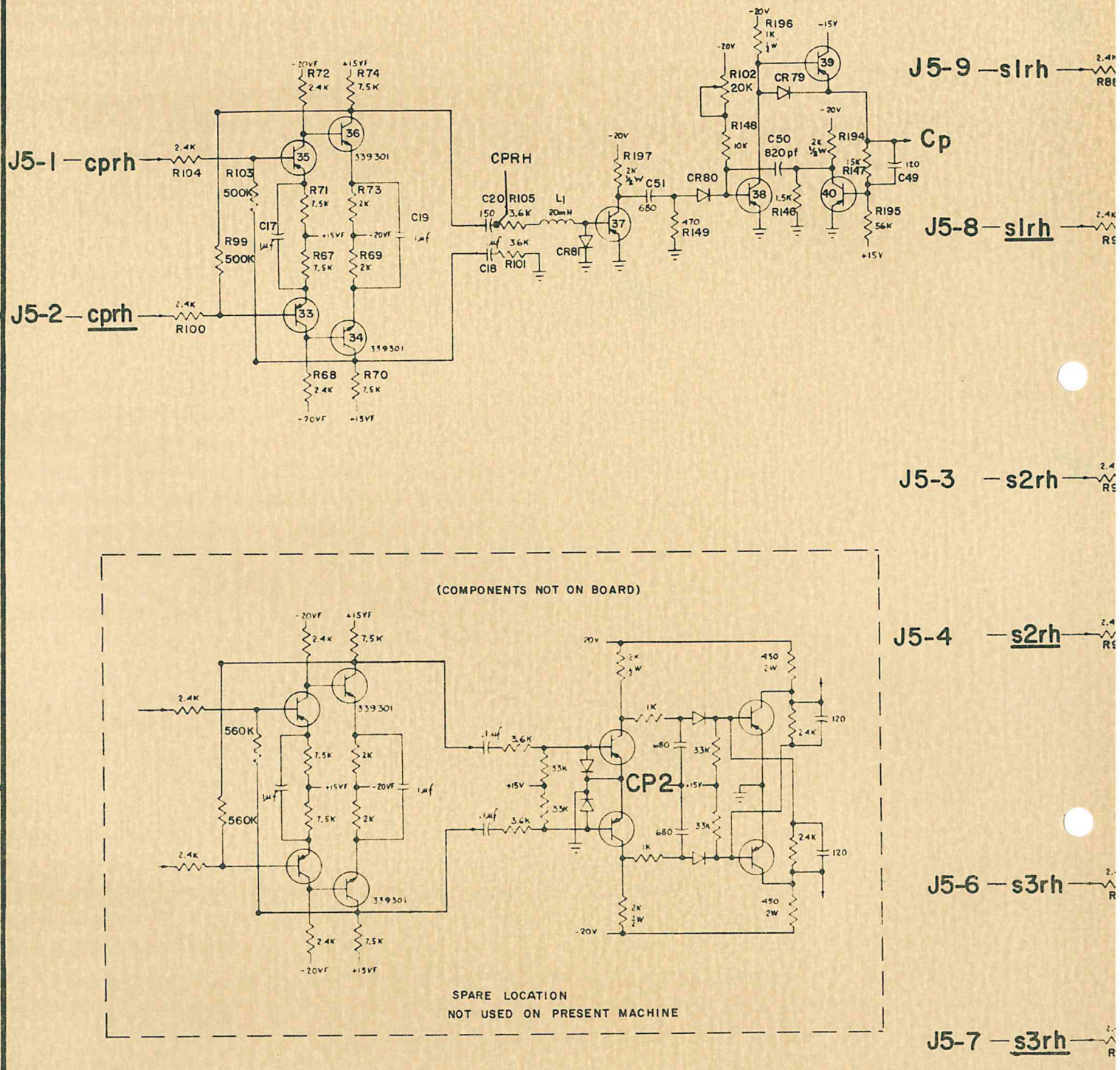
Memory Control # 1

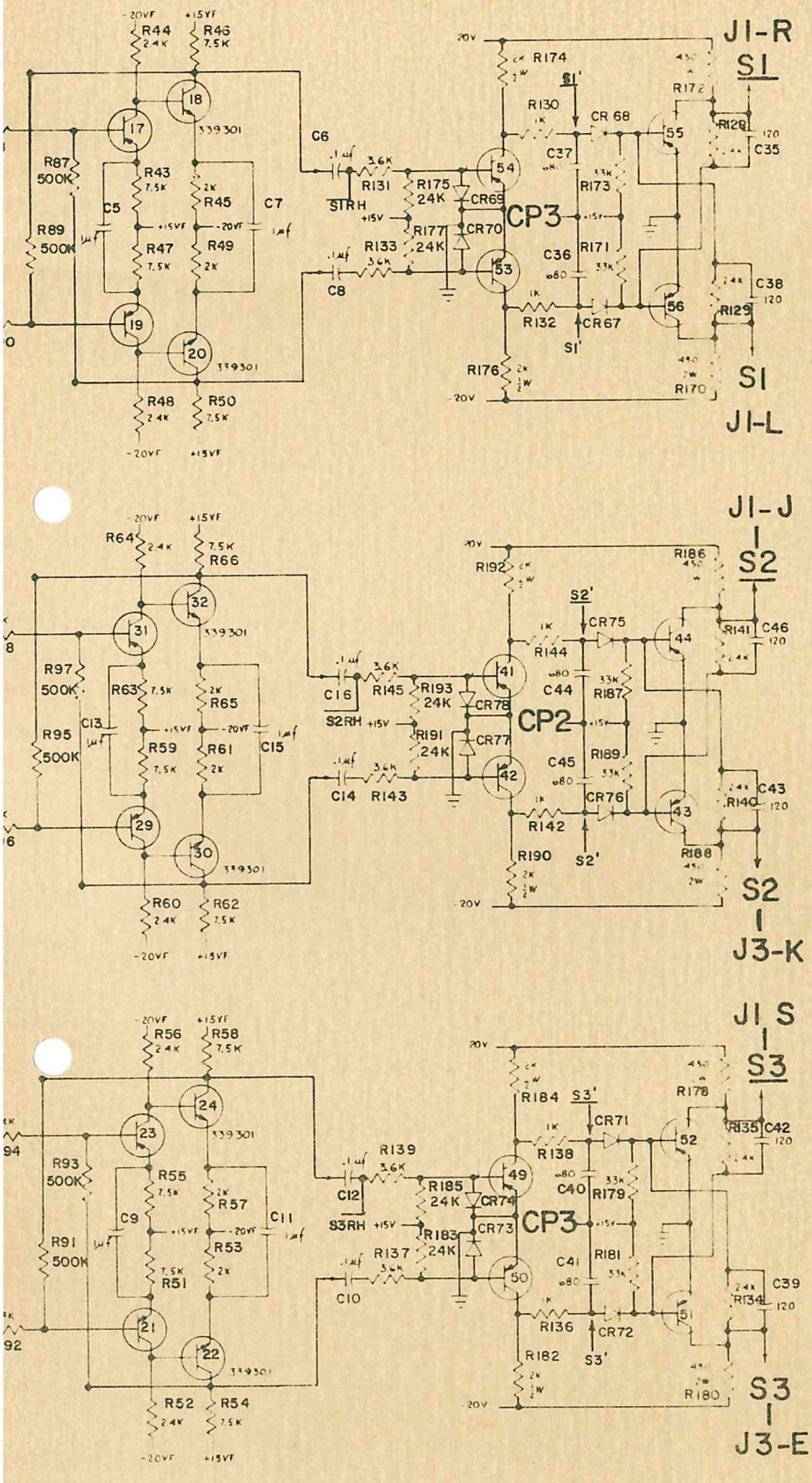
6-3

links


J1-Z
J4-3 J4-6 J4-2 J4-1 J4-5 J4-4 J4-8 J4-7
Vr2 Vr2 Vr3 Vr3 Vr4 Vr4 Vr1 Vr1
R8
R5
R16
R11
R24
R21
R32
R29
CR2
CR1
CR4
CR3
CR6
CR5
CR8
CR7
-20
R40 2.4K
R41 2K
R83 7.5K
R84 680K
R39 7.5K
R42 7.5K
R35 7.5K
R38 7.5K
R85 7.5K
R86 680K
R36 2.8K
R37 2K
C1 1uf
C3 1uf
C4 .01uf
C2 .01uf
W
VRH
+15
15pf
C34
10K
R127
R169 10K
CR CR 65 64
IN751A 5.1v
CR66
R125 3.6K
R124 3.6K
6.3v
R168 450 2W
R165 33K
R167 33K
R164 450 2W
R160 450 2W
R123 3.6K
C33 120
R121 24K
R122 3.6K
C32 120
R126 2K
CR62
CR63
VCP
INHIBIT BIT
C31 120
33K R163
+15K
V
-20y
58
59
60
61
62
13
14
15
16
57
63
64
65
66
450 -20V R159
C30 120
2.4K R118
450 -20V R161
C27 120
2.4K R117
R160 33K
CR60
CR61
R162 33K
1k R120
680 C28
680 C29
1K R119
CP3
R115 270
C26 120
7.5K R116
15K R158
+15V
-20d
R198 150Ω ½W
IN751A 5.1V ± 5%
CR53
450Ω 2W
R106
CR51
IN3018B 8.2V ± 5%
-10V
-2V
SC-2 CR52
SC-2 CR54
SC-2 CR55
-20V
R156 800 2W
C25 120 pf
6.8K ¼W R114
56K ¼W R157
+15V
MEMORY CONTROL
ESD-1060
PAGE 1 OF 3

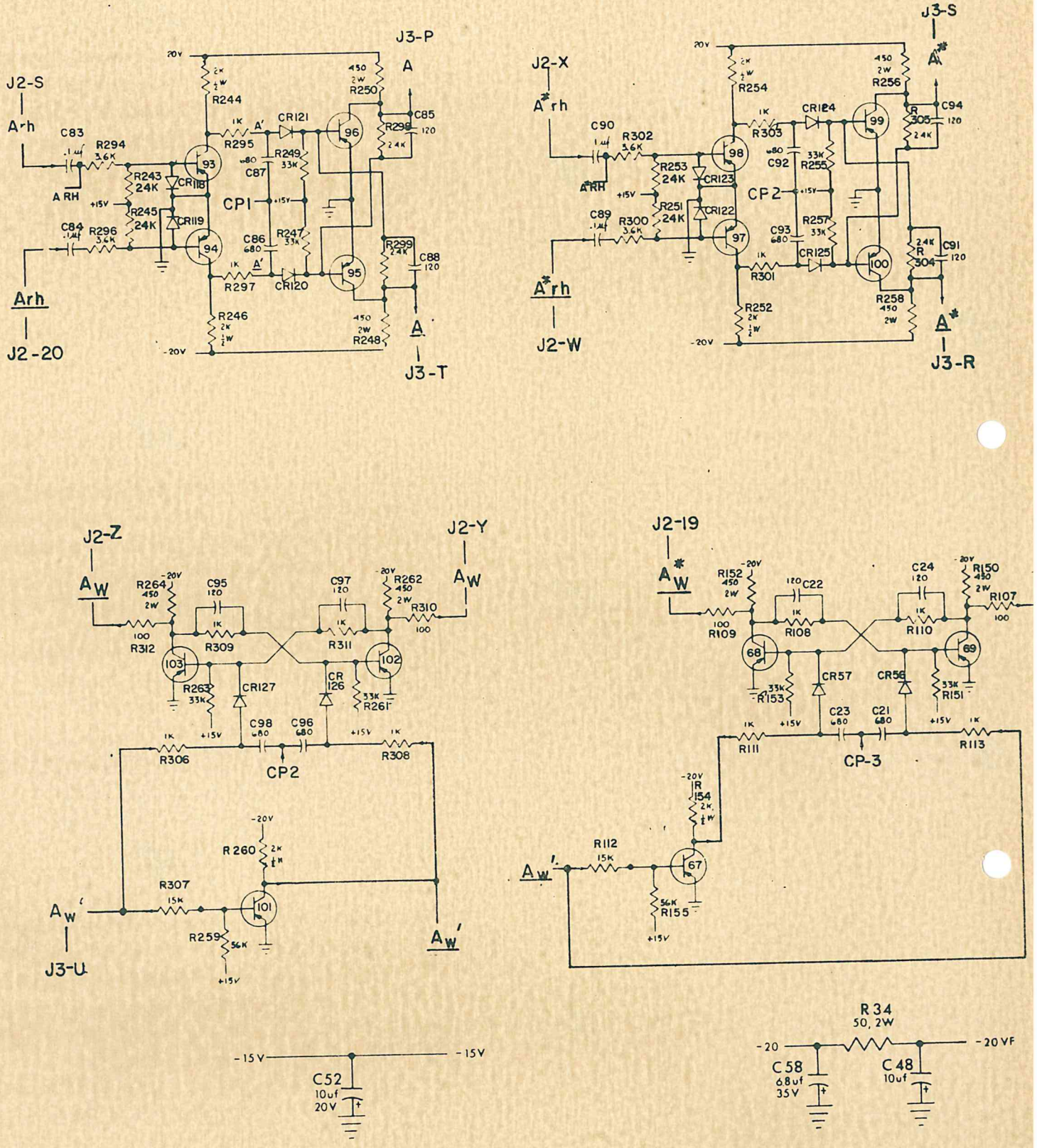
techs.


J5-1 — cprh
J5-2 — cprh
J5-9 — s1rh
J5-8 — s1rh
J5-3 — s2rh
J5-4 — s2rh
J5-6 — s3rh
J5-7 — s3rh
Cp
CPRH
CP2
(COMPONENTS NOT ON BOARD)
SPARE LOCATION
NOT USED ON PRESENT MACHINE



MEMORY CONTROL
ESD-1060
PAGE 2 OF 3

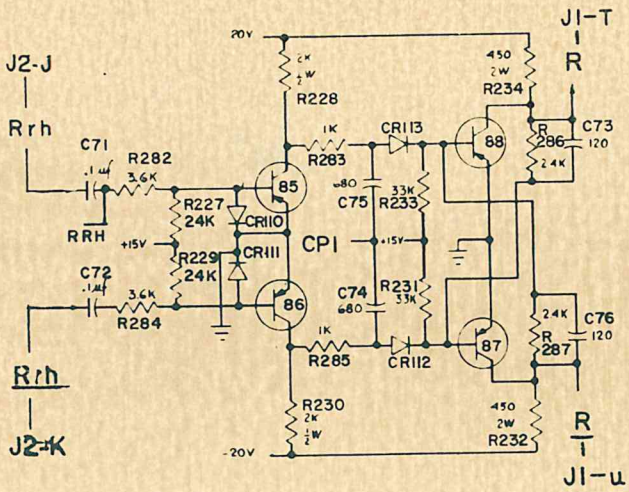
rechh

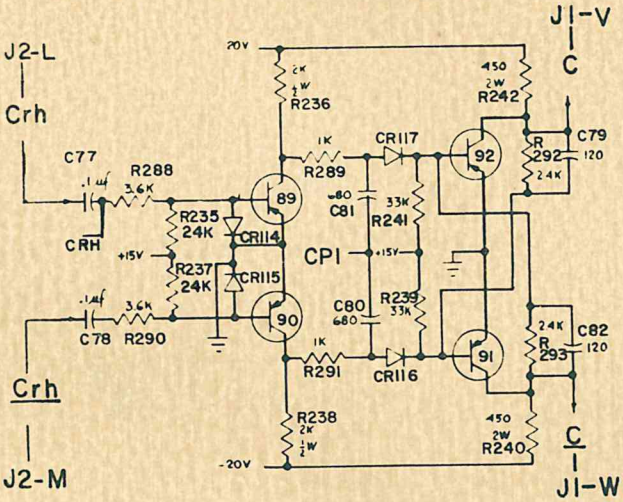


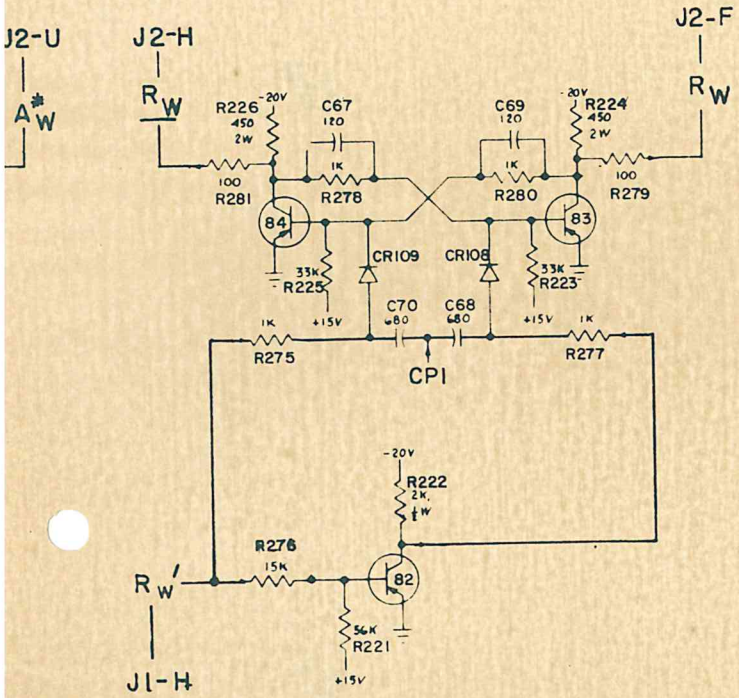
Revised March, 1964

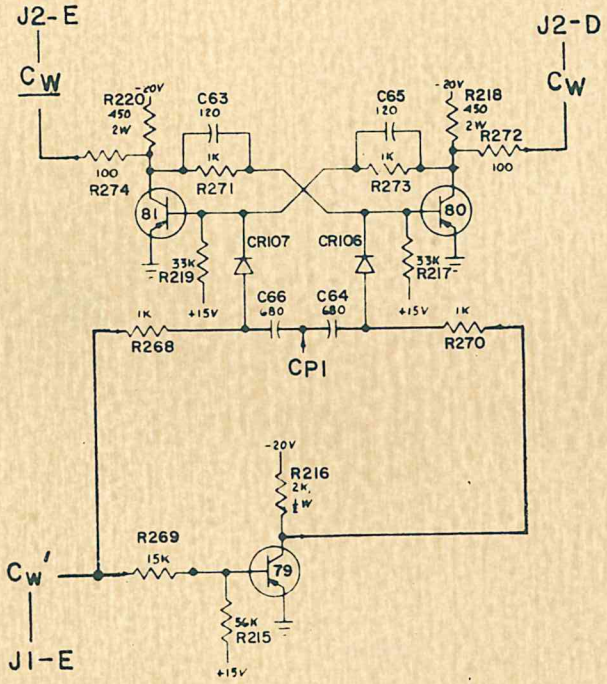
6-7 Memory control 3

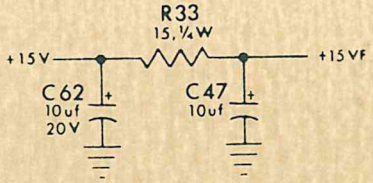
links.











MEMORY CONTROL

ESD-1060

PAGE 3 OF 3

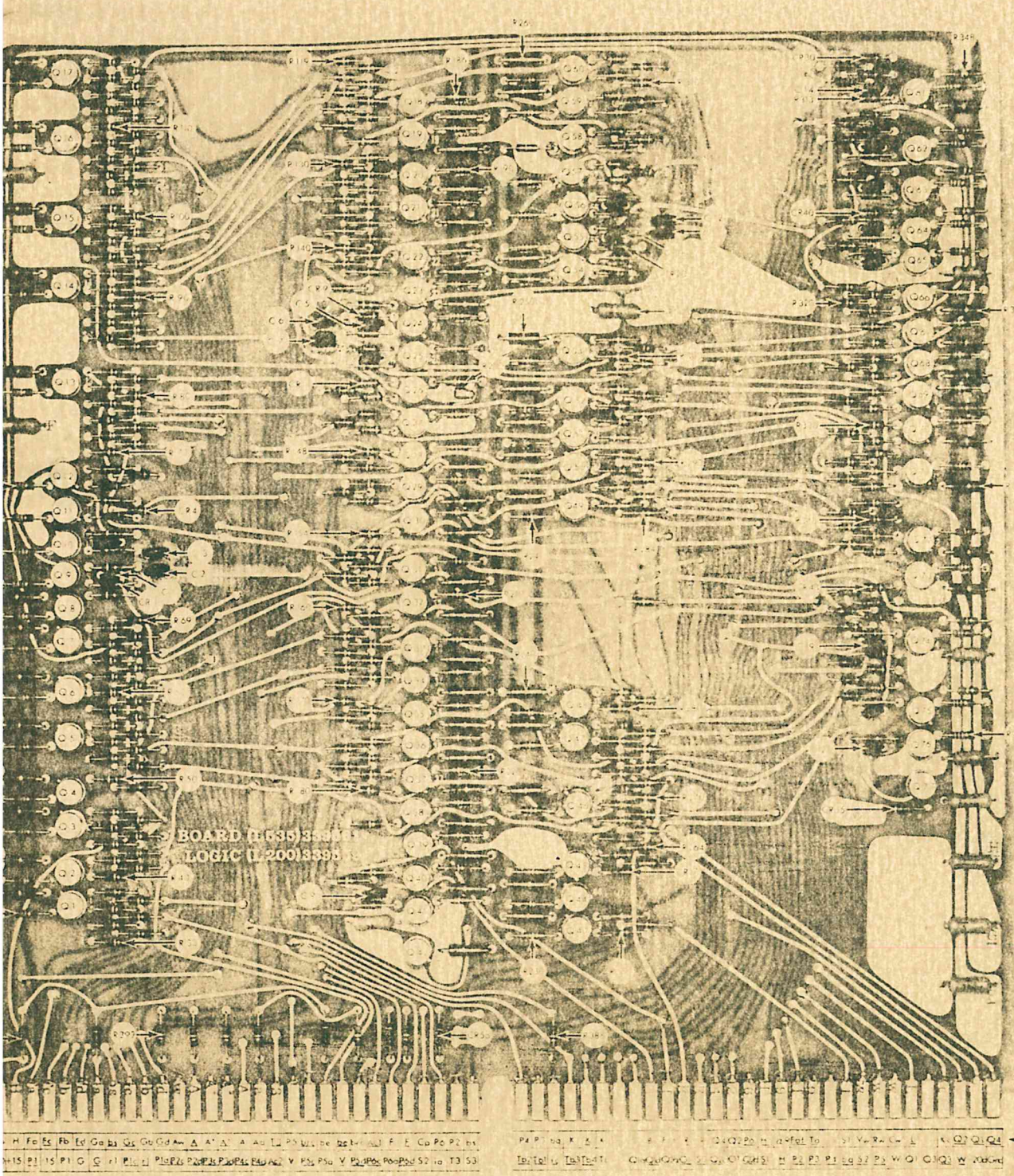
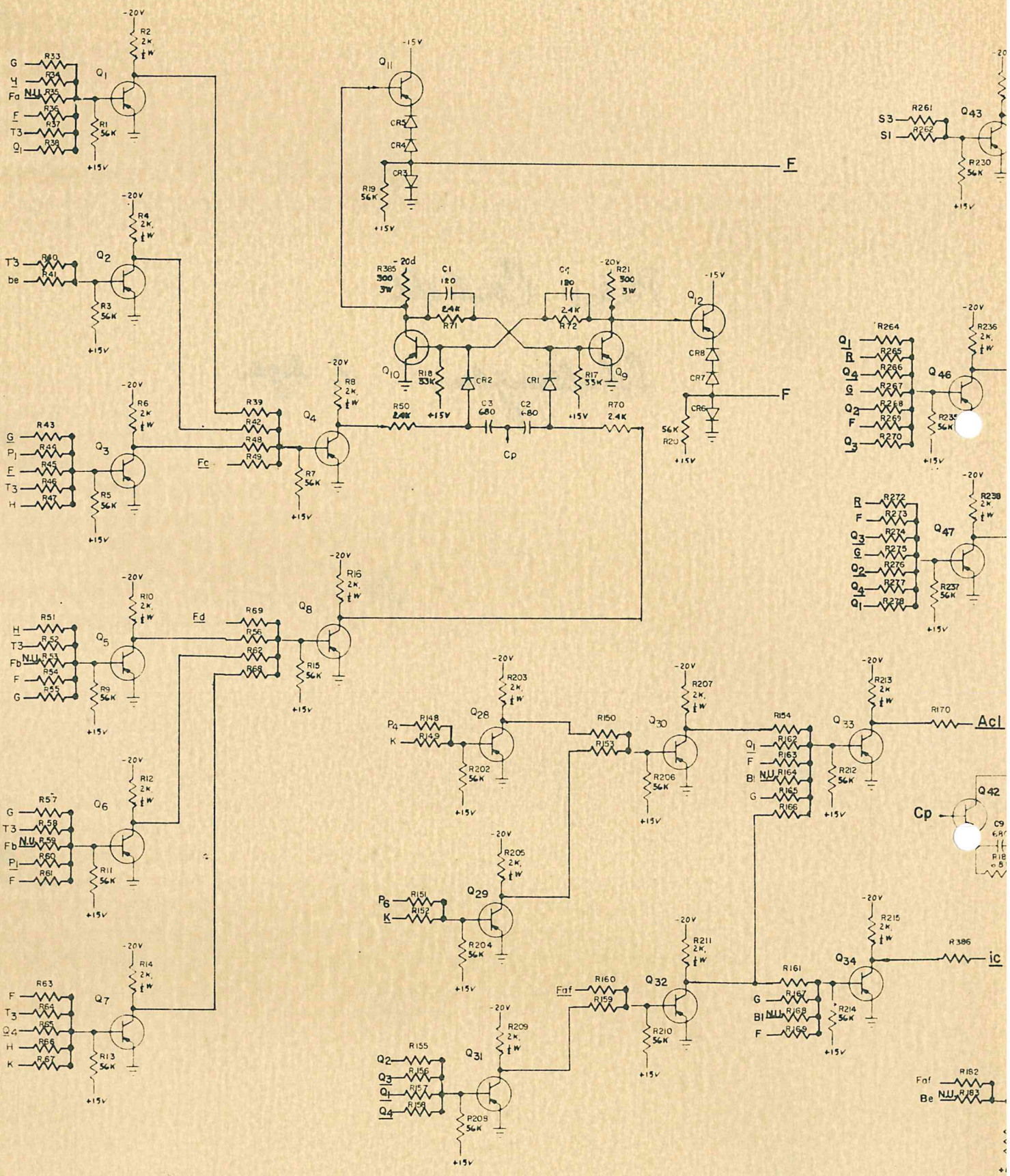


FIGURE 6-4 PHASE CONTROL BOARD

Phase Control

Schaltungen 2 Bogen

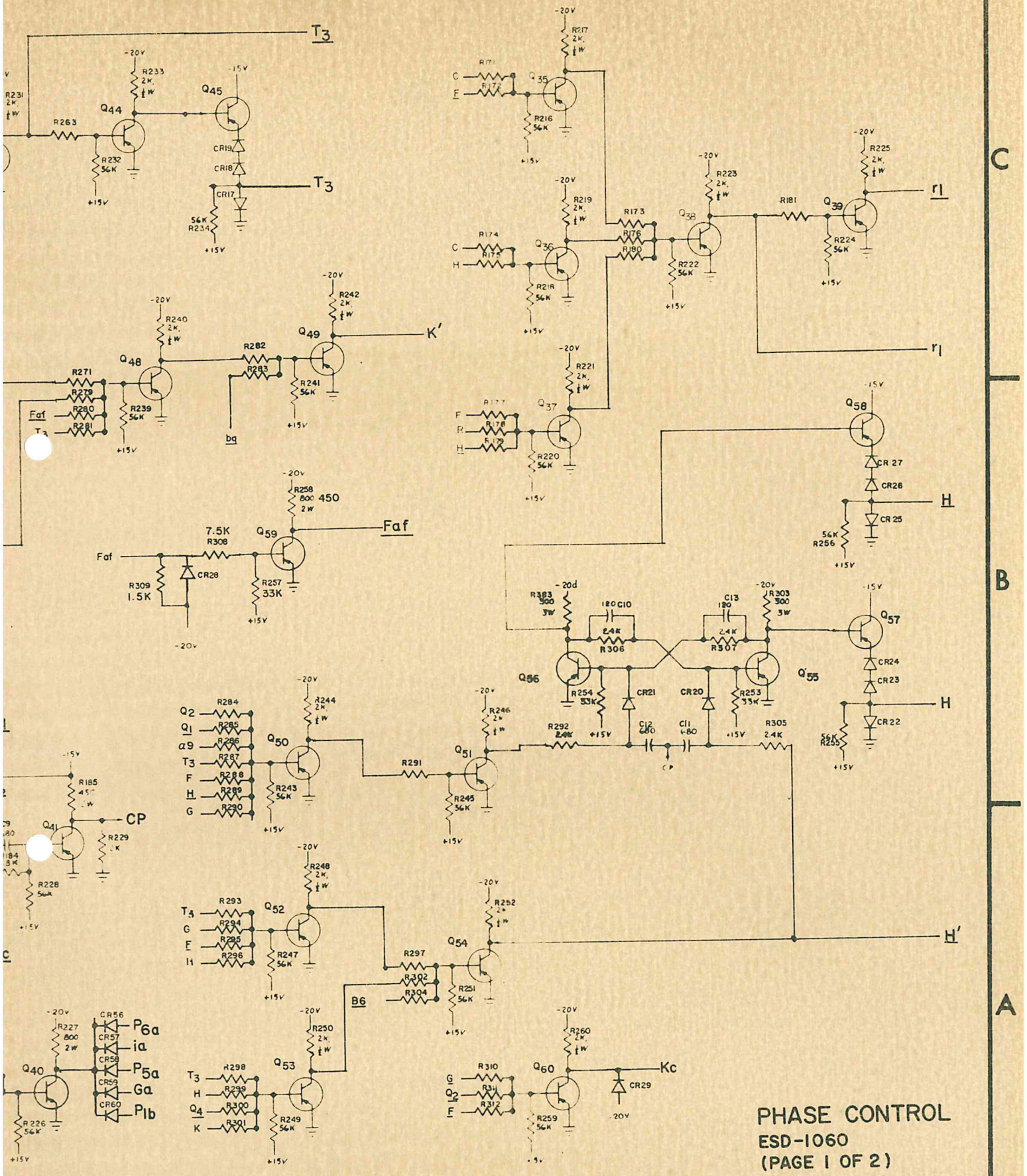


Revised March, 1964

Phase Control 1

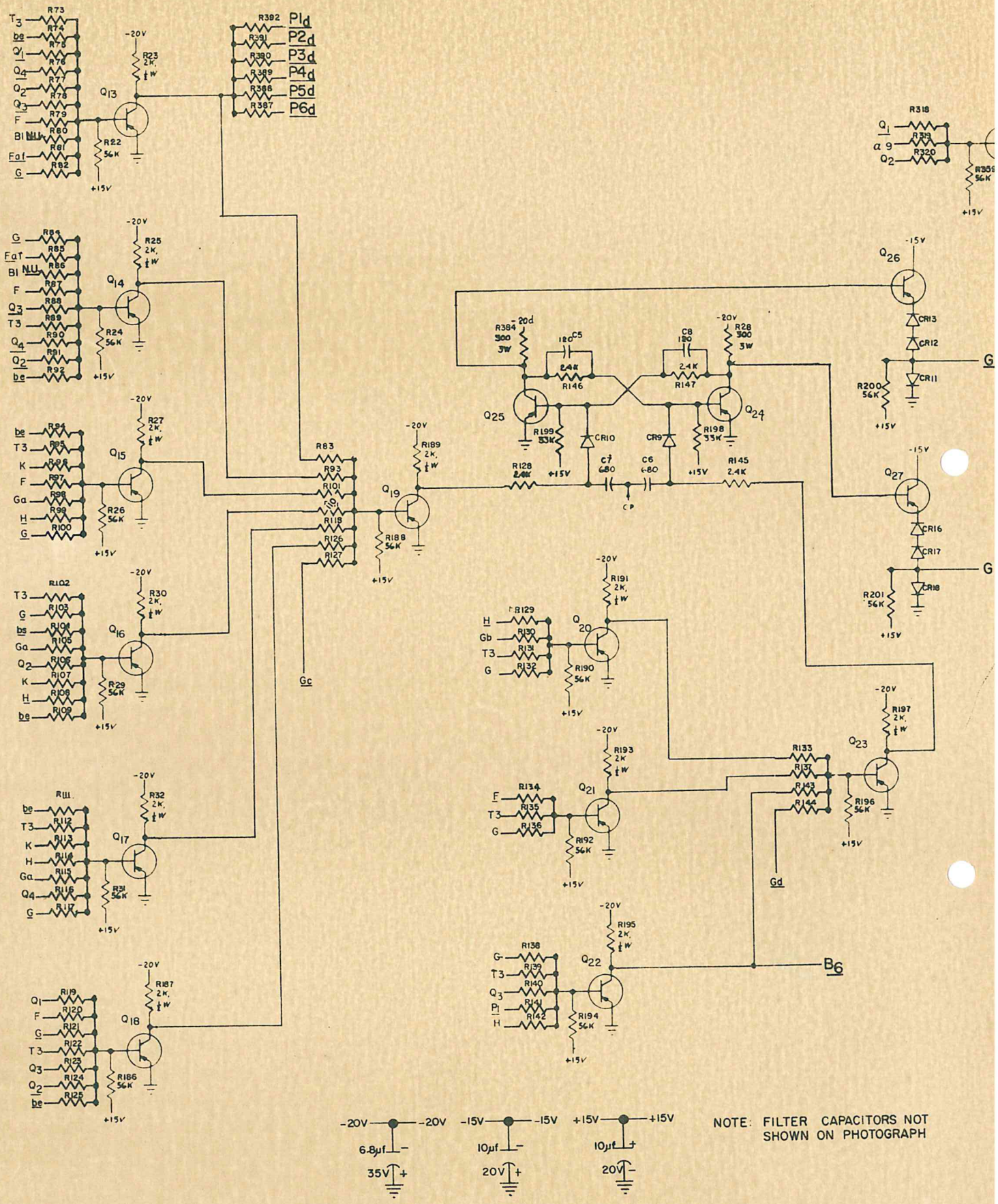
6-9

links



PHASE CONTROL
ESD-1060
(PAGE 1 OF 2)

rechs

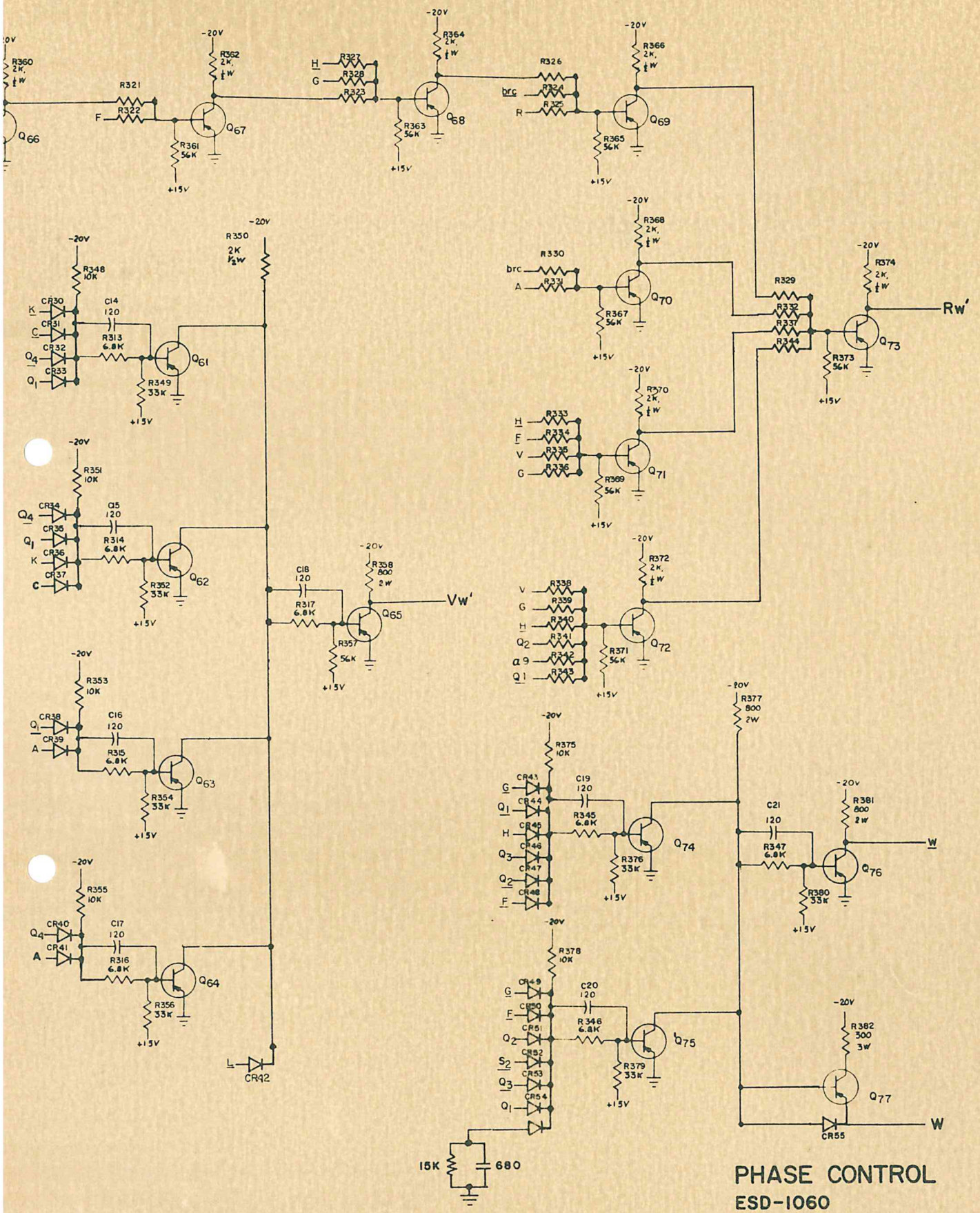


Revised March, 1964

Phase Control 2

6-11

links



PHASE CONTROL

ESD-1060

(PAGE 2 OF 2)

rechb

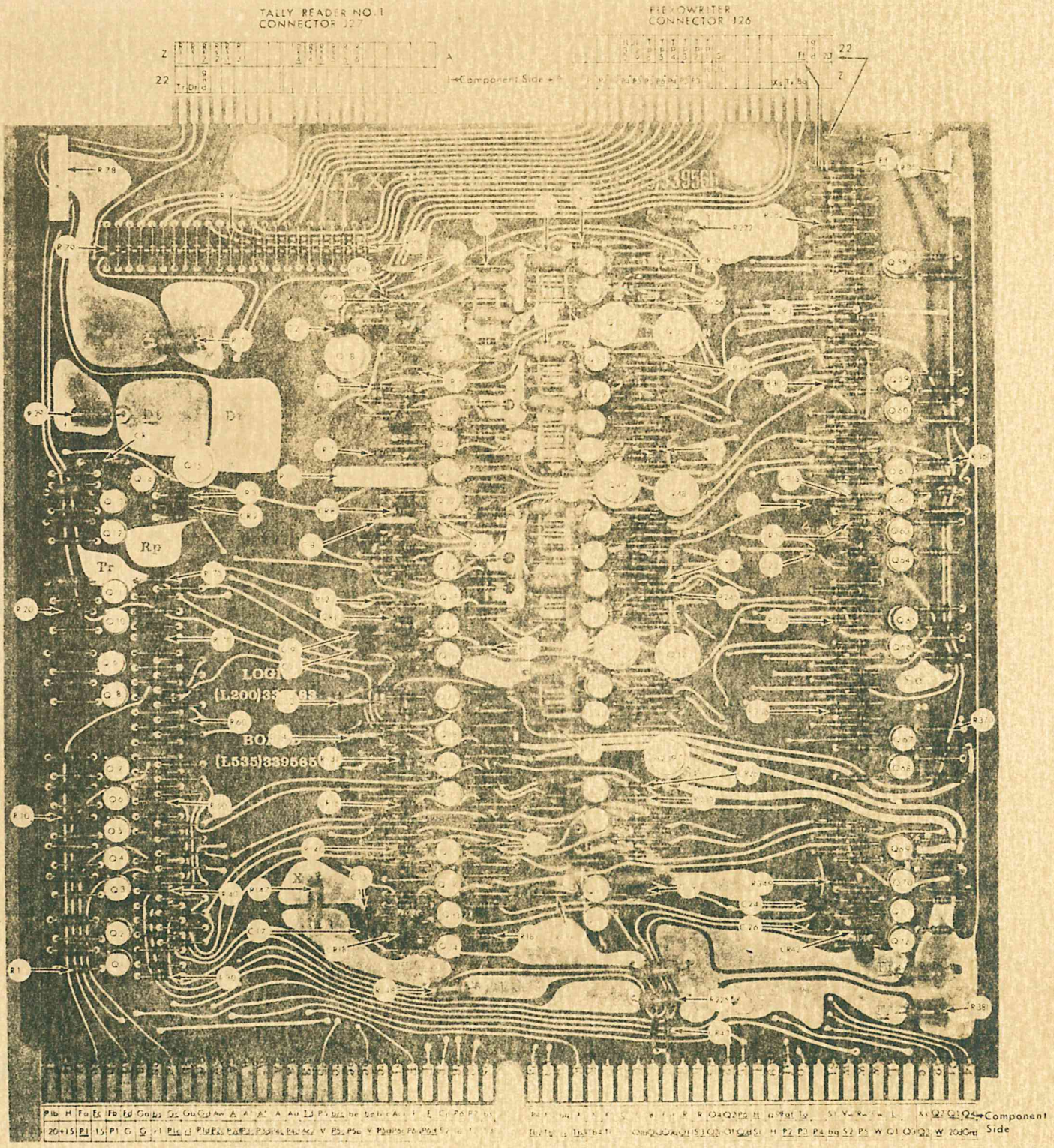


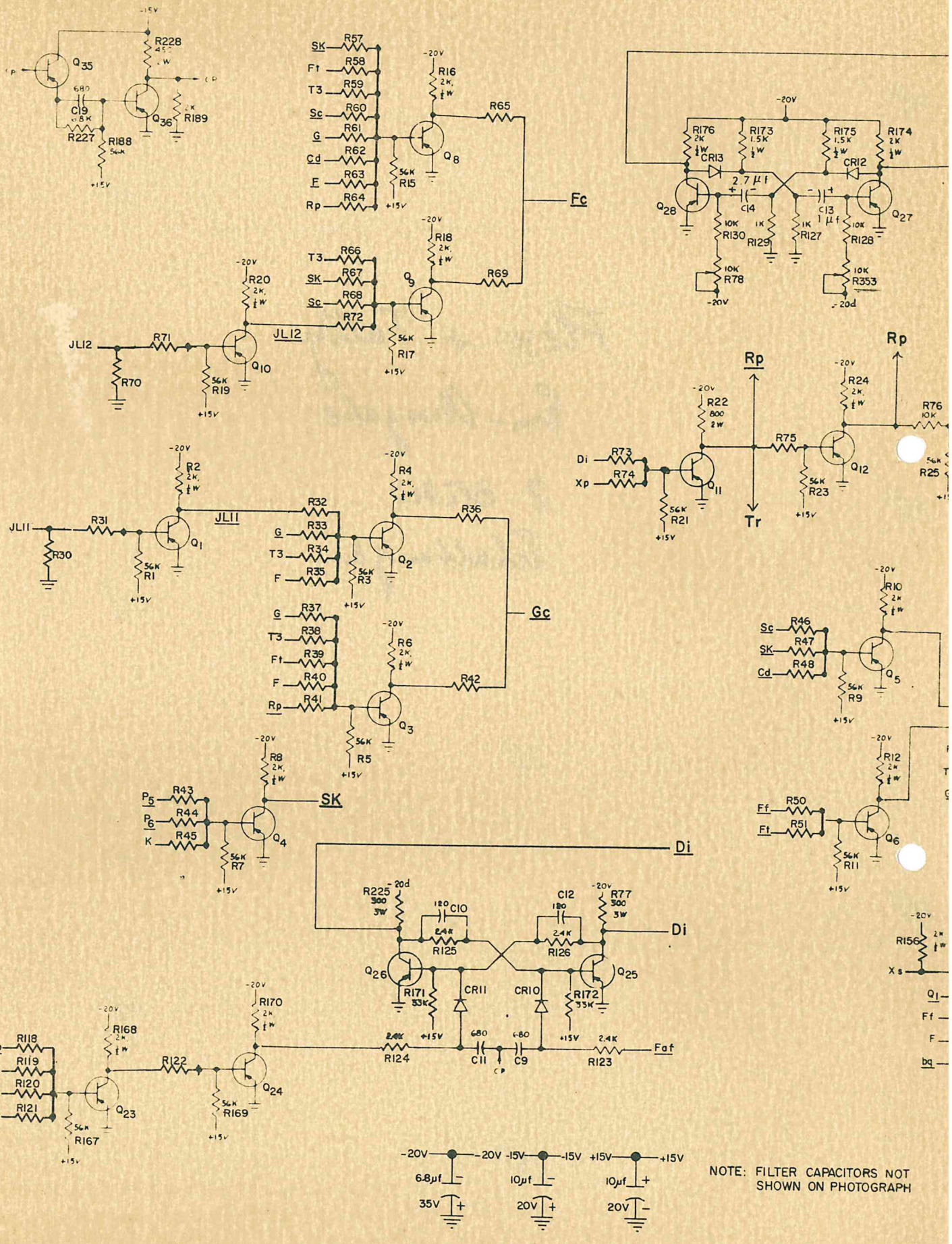
FIGURE 6-6 FLEX-TALLY I/O BOARD

Flex + Tally

Ein-Ausgabe

2. Blätter

Schaltungen

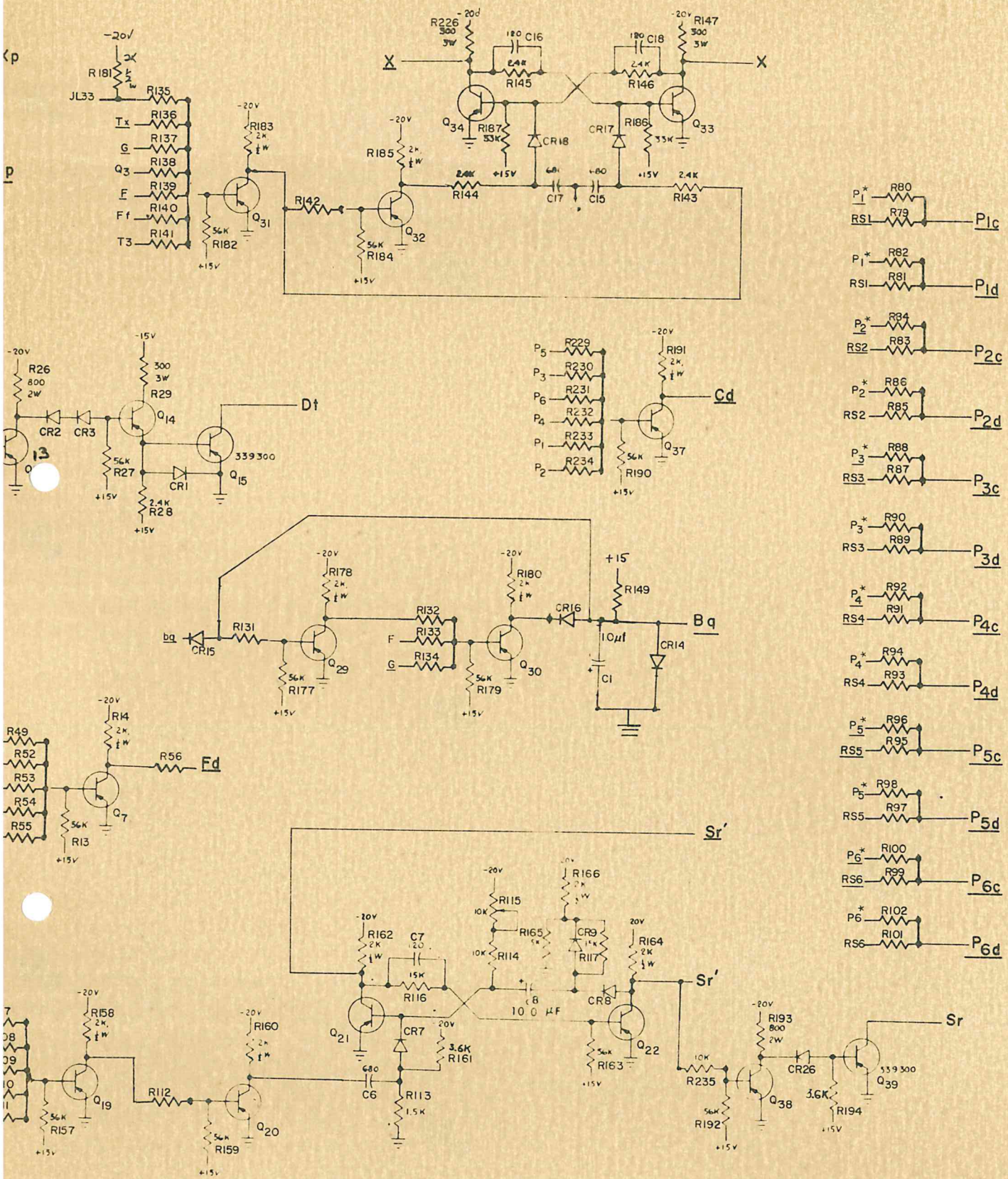


Revised March, 1964

Flex Tally 1/0

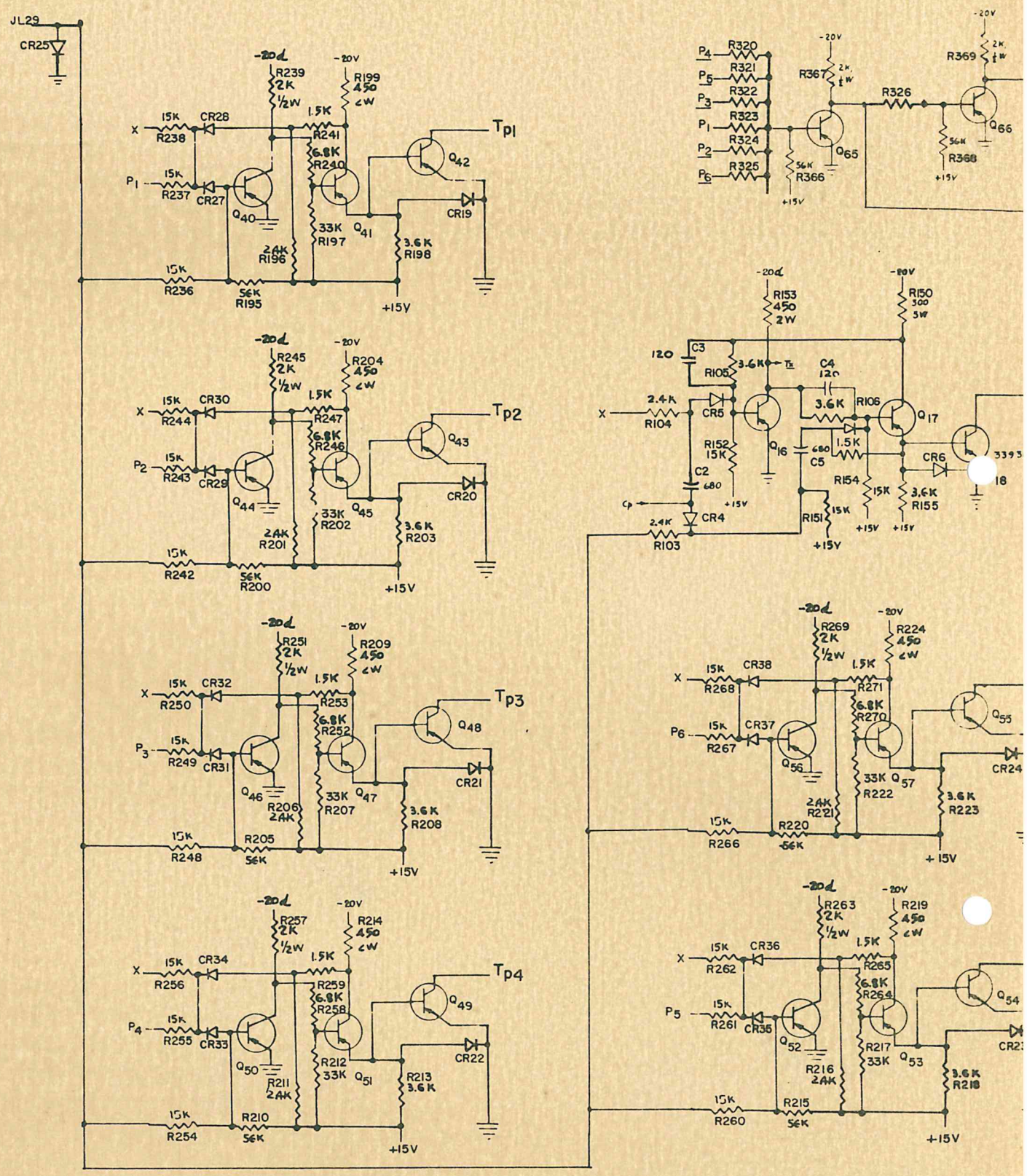
6-13

links



FLEX-TALLY I/O
ESD-1060
(PAGE 1 OF 2)

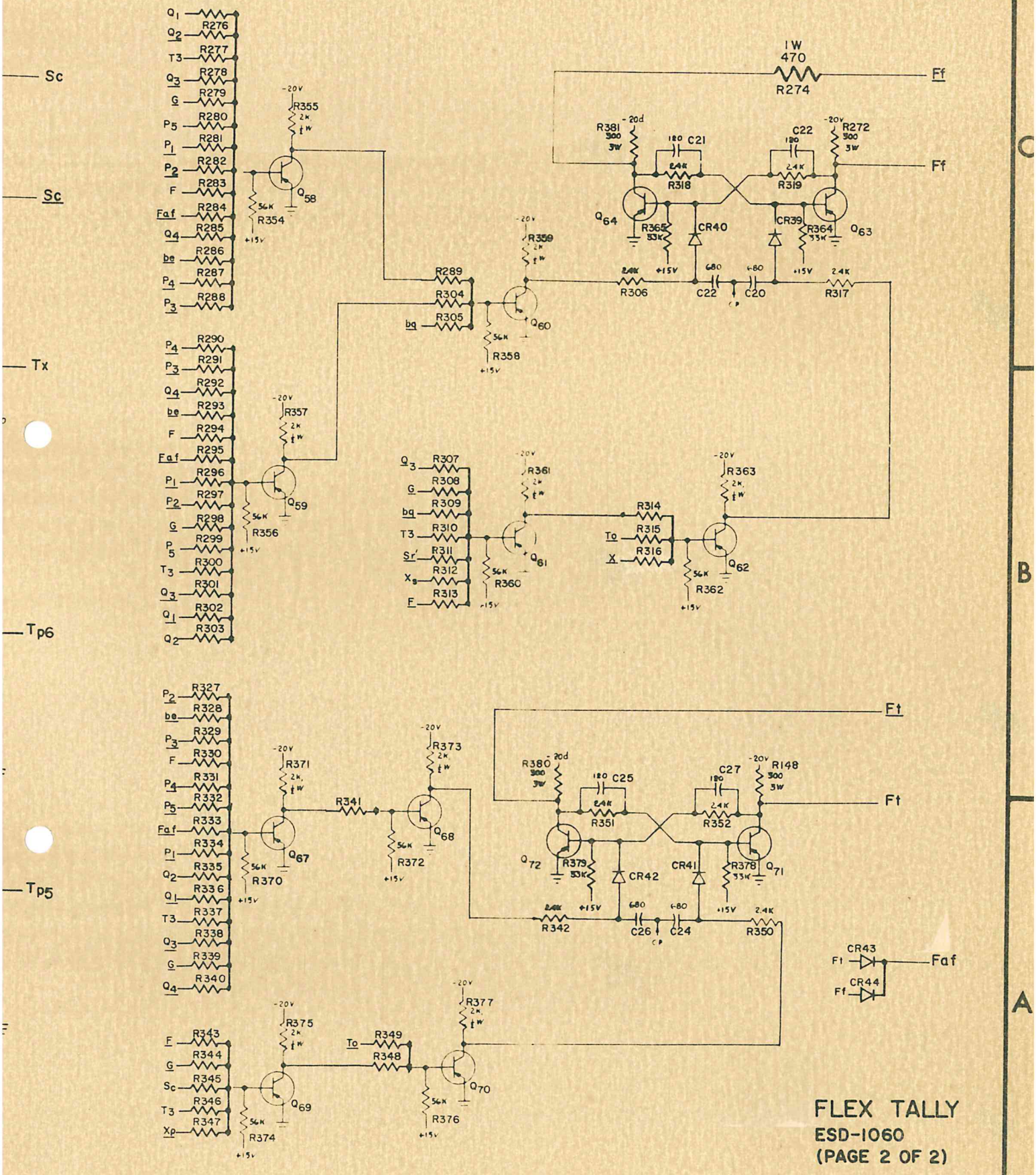
rechh.



Revised March, 1964

6-15

Flex Tally 2



FLEX TALLY
ESD-1060
(PAGE 2 OF 2)

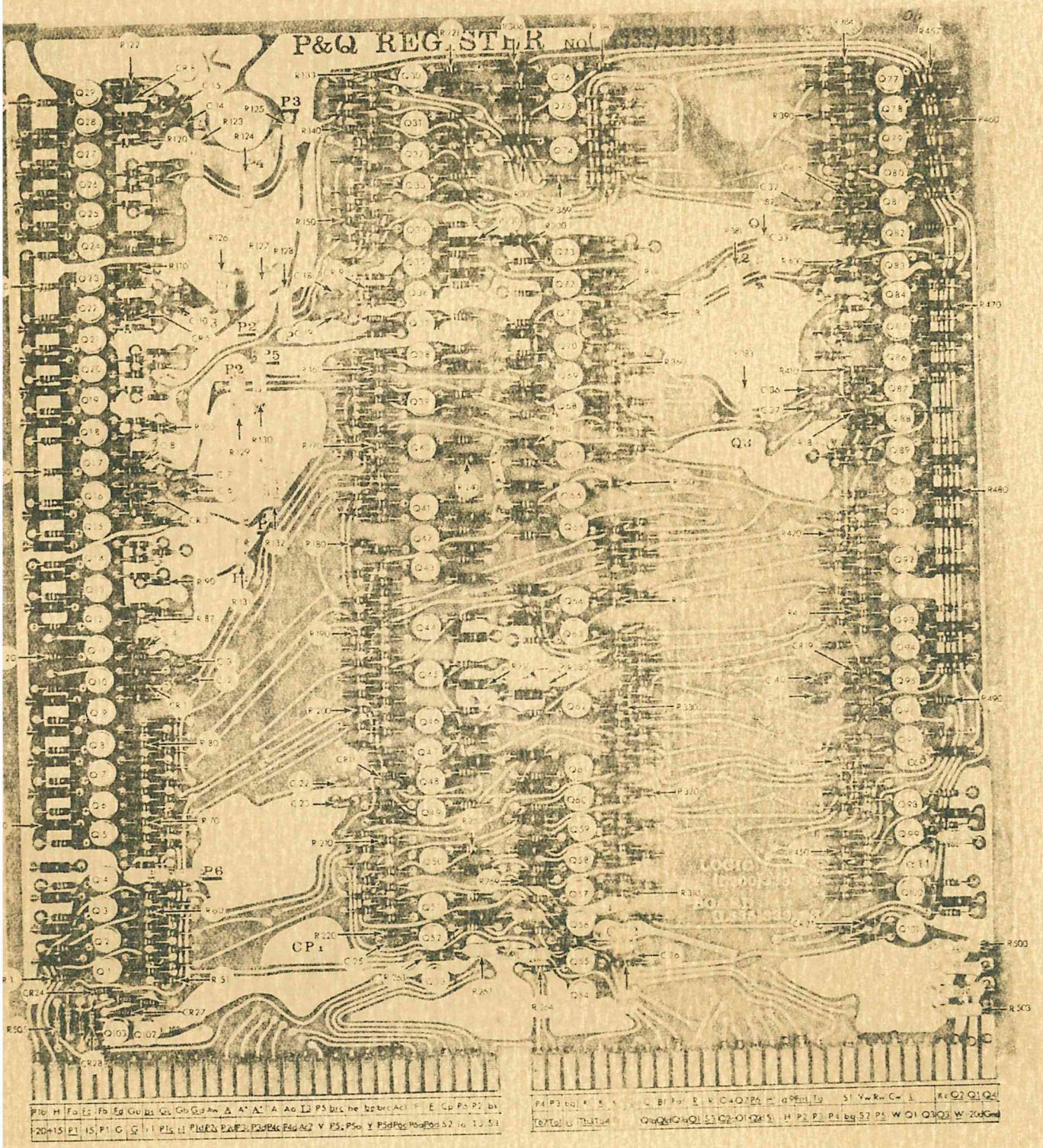


FIGURE 6-10 P AND Q REGISTER BOARD

P u. Q Register

Schaltungen

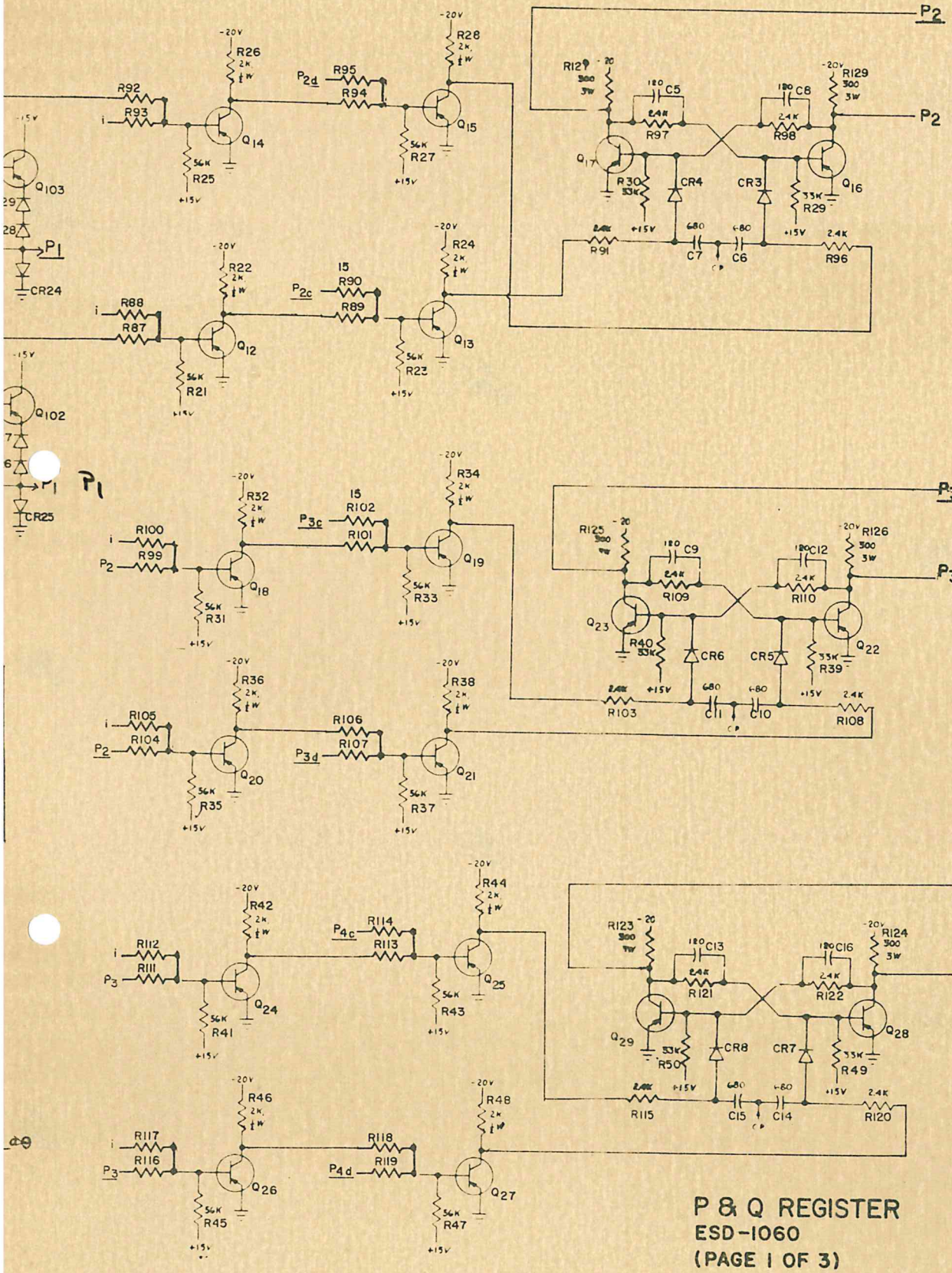
3 Blatt

Revised March, 1964

P&Q Register links

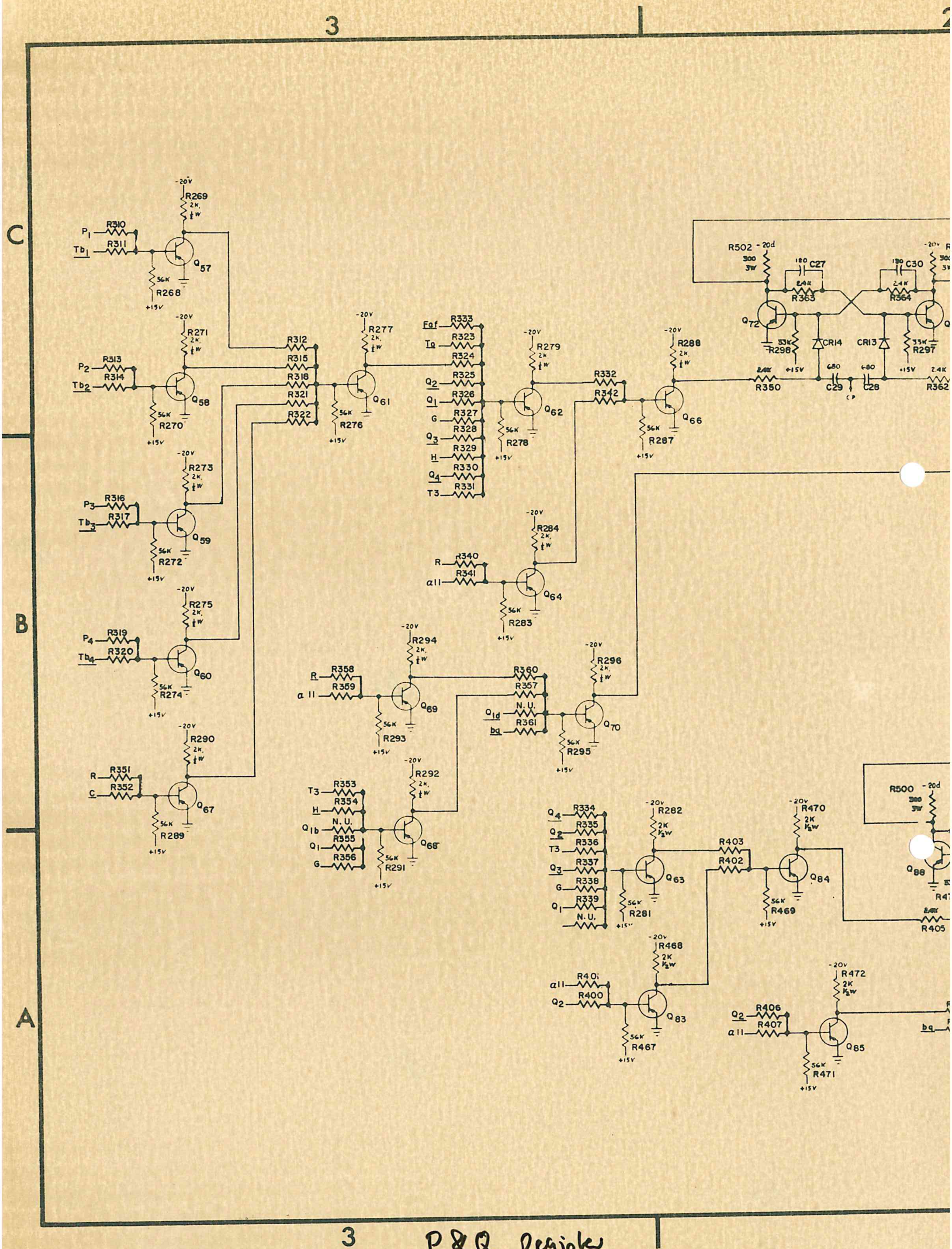
1. (von 3)

6-1221



P & Q REGISTER
ESD-1060
(PAGE 1 OF 3)

rechb.



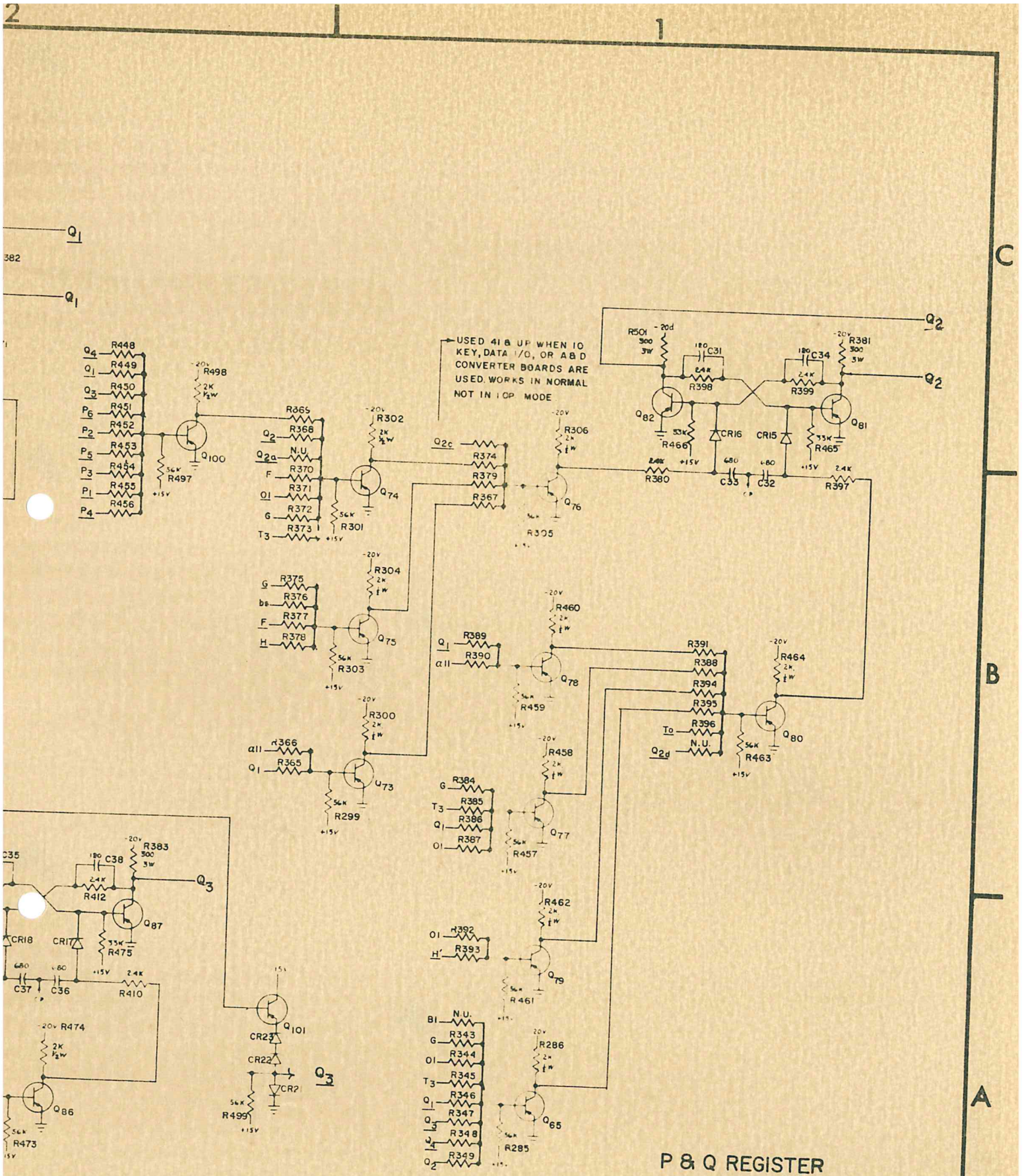
Revised March, 1964

6-23

P & Q Register

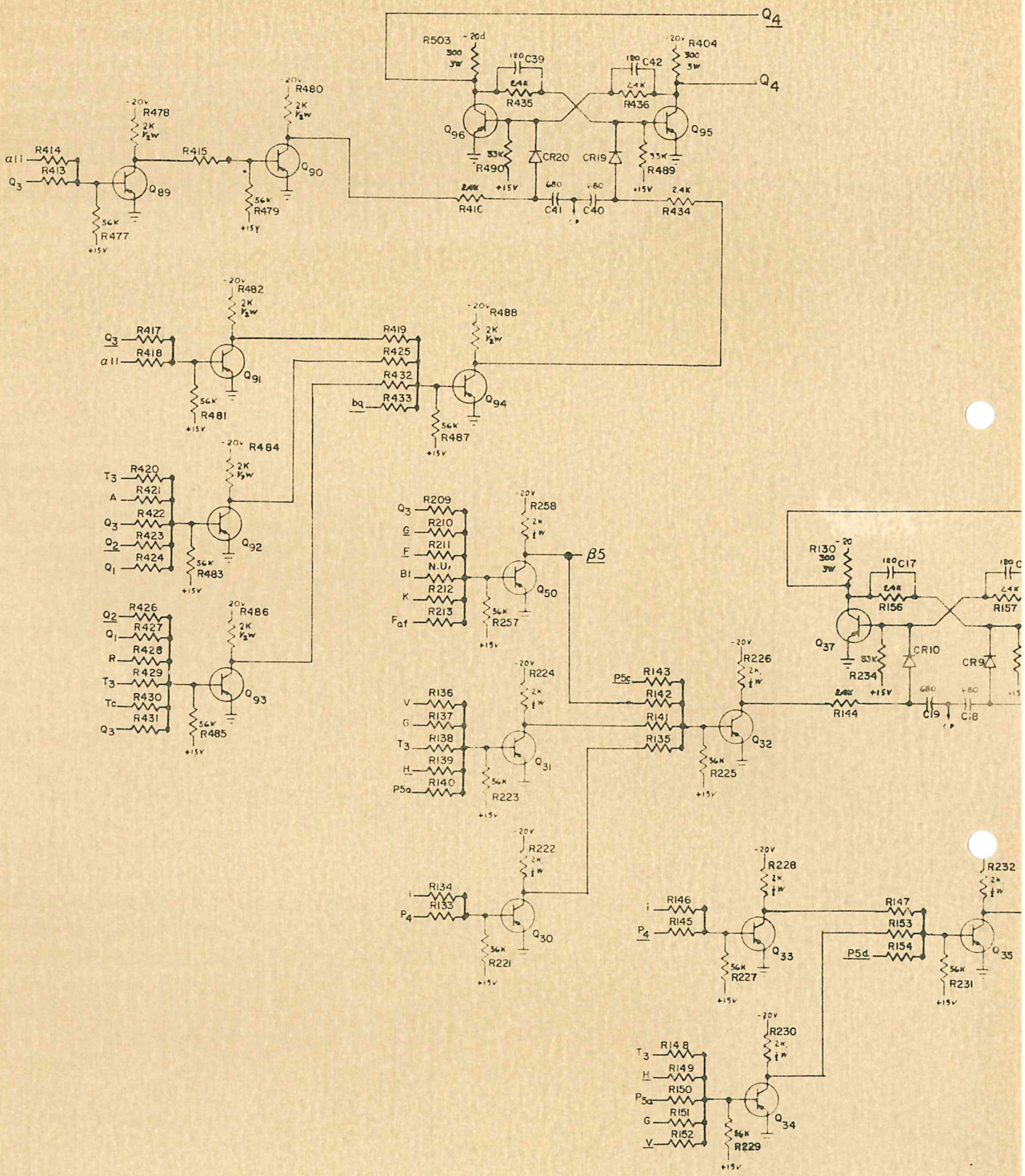
2. von 3

links



P & Q REGISTER
ESD-1060
(PAGE 2 OF 3)

rechs.

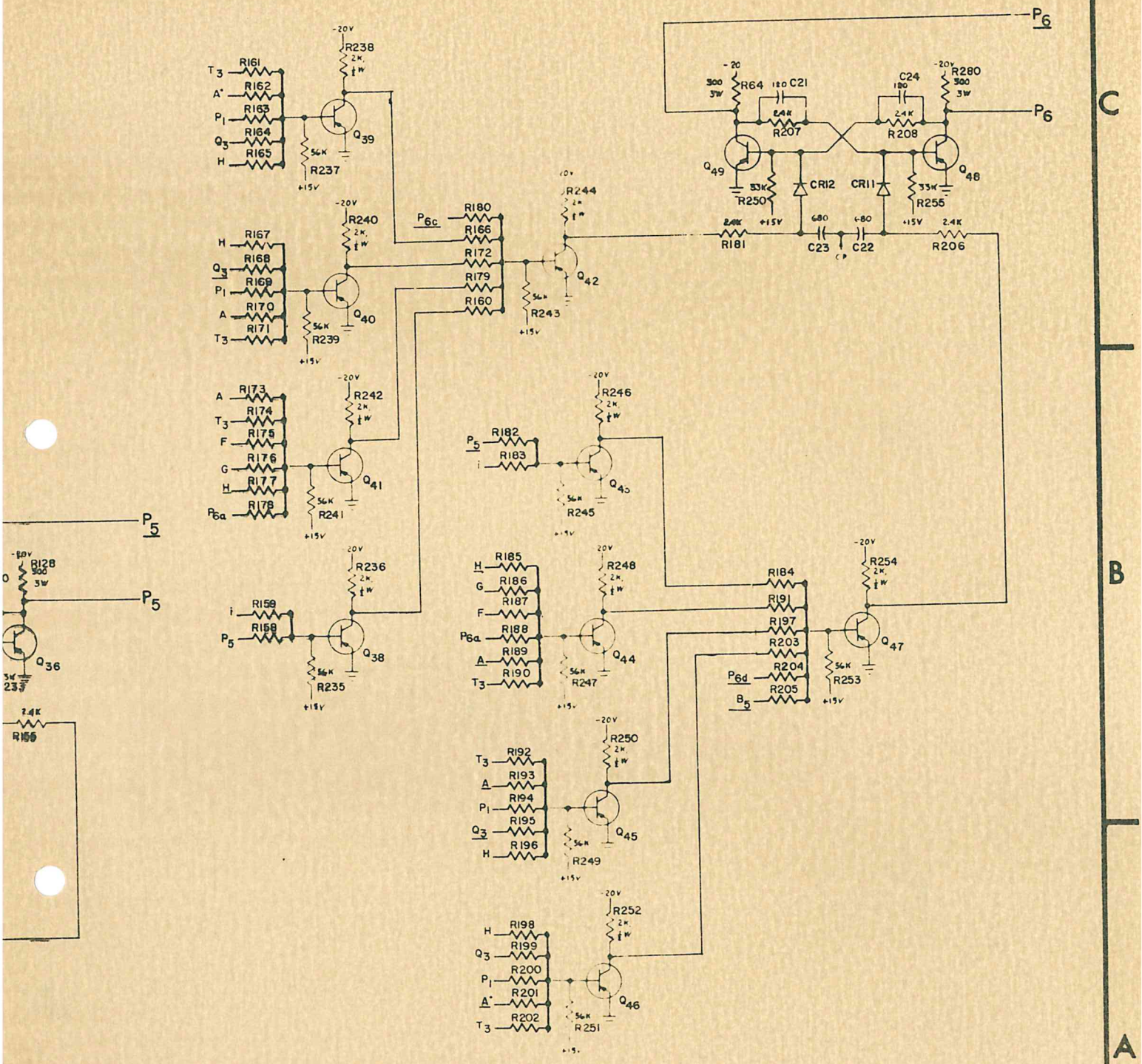


Revised March, 1964

P & Q Register 3

G-25

links



P & Q REGISTER
ESD-1060
(PAGE 3 OF 3)

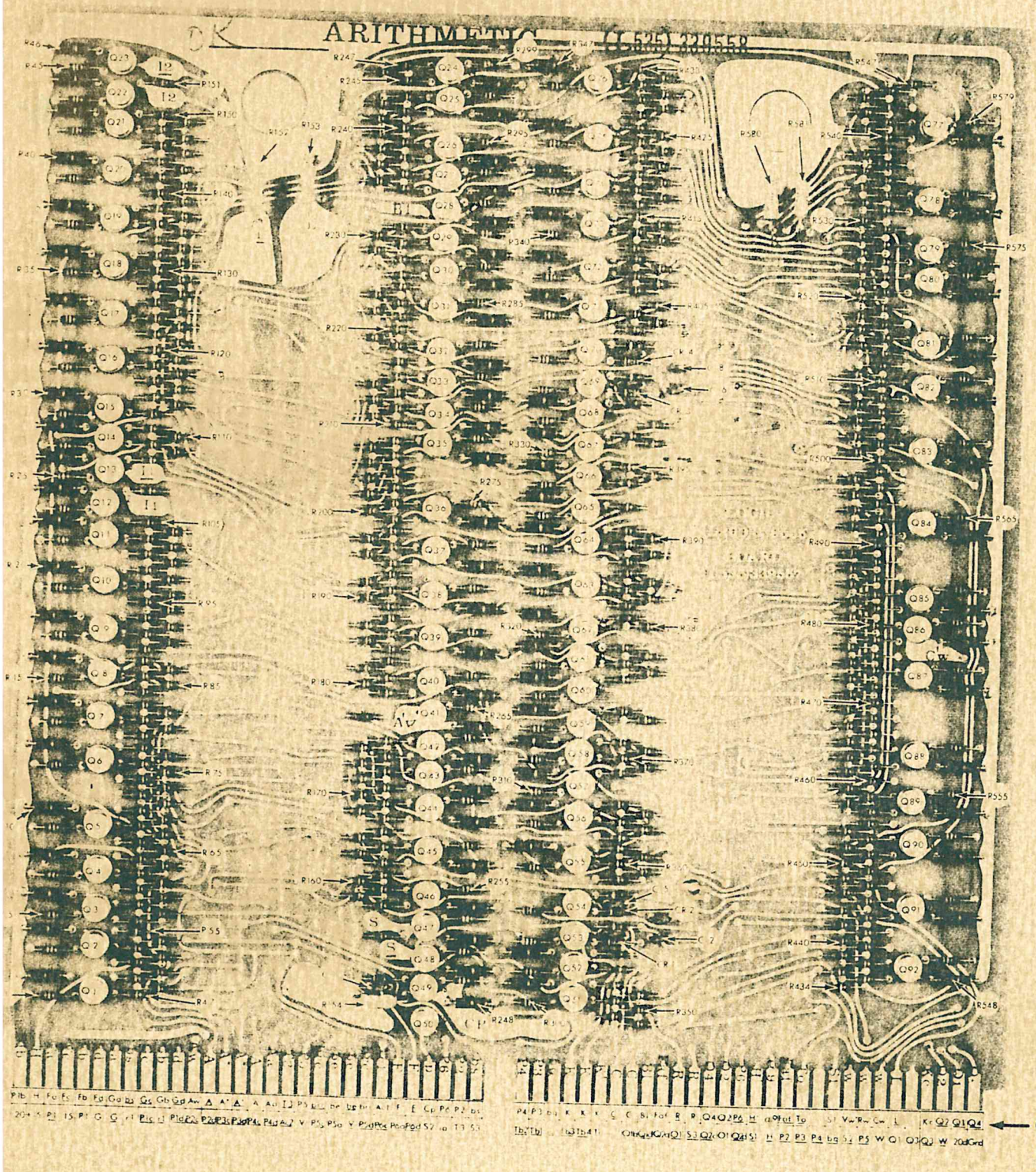


FIGURE 6-14 ARITHMETIC BOARD

Section 8

Complete Parts List

SECTION VIII

COMPUTER PARTS LIST

PREFACE

The following parts list and illustrations cover the spare parts for the LGP-21 Computer that are available from the Parts Department. This list covers the service parts that will be required for field replacement needs for the main frame.

TRANSISTORS

Part Number	Description	Type	Mfg.	
339 108	Transistor	PNP	GRM.	T1-N652
339 301	Transistor	NPN	GRM.	2N-1308
L532 000 803	Transistor	NPN	Sil	T1-486
339 300	Transistor	PNP	Pwr	2N1183B

DIODES

339 178	Diode	Fast Recovery Silicon	
L531 000 807	Diode	Controlled Fwd Drp. Silicon	
339 263-1	Diode	SC-2	
L531 000 813	Diode	Zener Sil. 5.1V	1N751A
L531 000 802	Diode	Zener Sil. 8.2V	1N1318B
339 264	Diode	Rectifier Sil	1N1200A

CAPACITORS

339 325-1	Capacitor	32,000 mf.	25V
339 324-2	Capacitor	3600 mfd.	20V
339 324-1	Capacitor	2300 mfd.	20V
339 325-2	Capacitor	1600 mfd.	75V
L605 009 006	Capacitor	18 mfd.	100V
339 376-4	Capacitor Tant.	10 mfd.	20V
339-376-3	Capacitor Tant.	2.7 mfd.	20V
339 376-1	Capacitor Tant.	1.0 mfd.	20V
339 105-1	Capacitor	1.0 mfd.	200V
339 320-21	Capacitor Ceramic	1.0 mfd.	25V
339 320-1	Capacitor Ceramic	.1 mfd.	25V
L605 009 002	Capacitor Ceramic	.01 mfd.	50V
L605 009 005	Capacitor Ceramic	680 PF	
L605 009 004	Capacitor Ceramic	150 PF	
L605 009 003	Capacitor Ceramic	120 PF	
339 358-1	Capacitor Oil	2 mfd.	256V AC
339 359-1	Capacitor	6 mfd.	330V AC

RESISTORS

339 307-21	Resistor	10K	Variable
339 316-91	Resistor	56K 1/4w	5%
339 316-85	Resistor	33K 1/4w	5%
339 316-77	Resistor	15K 1/4w	5%

Part Number	Description	Type	Mfg.
339 316-73	Resistor	10K 1/4w 5%	
339 316-69	Resistor	6.8K 1/4w 5%	
339-316-58	Resistor	2.4K 1/4w 5%	
339-316-49	Resistor	1K 1/4w 5%	
339 316-5	Resistor	15 OHMS 1/4w 5%	
L600 090 501	Resistor	2K 5w	
L600 090 502	Resistor	1K 10w	
339 219-10	Resistor	300 OHMS 3w	
339 305-7	Resistor	450 OHMS 2w	
339 305-4	Resistor	800 OHMS 2w	
L600 090 503	Resistor	10K 1/8w 1%	
L603 000 829	Resistor Thermistor Fenwal Ka31L1		

MEMORY UNIT

L200 013 729	Head assm. Main Memory 410 Turn
338 497	Head assm. Main Memory 460 Turn
L200 011 851	Head assm. 1 wd. Recirc.
L200 011 850	Head assm. 2 wd. Recirc.
338 465	Reed Main Memory Mounting Leaf Spring
338 466	Reed Recirc. Head Mounting Spring

RELAYS

339 357	Relay 115V AC 20 sec. Delay
L503 000 801	Relay Indicator Control (I/O - Start)
L503 000 805	Relay Motor Start
L200 013 679	Relay and Elapsed Time Meter Assm.
L503 339 357	Relay Meter Control
L512 000 801	Meter, Elapsed Time
L505 000 801	Relay, Circuit Breaker

WIRING HARNESS

L541 000 809	Wiring Harness Memory Matrix
L541 000 807	Wiring Harness Dist. Bd. to Power Supply
L541 000 806	Wiring Harness Control Panel
L541 000 804	Wiring Harness Display Conn. to Dist. Bd.
L542 000 830	Wiring Harness Tally Punch to I/O Card
L541 000 805	Wiring Harness Tally Reader to I/O Card
L541 000 803	Wiring Harness Flexo to I/O Card
L541 000 813	Wiring Harness Dist. to Memory Control J1
L541 000 814	Wiring Harness Dist. to Memory Control J3

CABLES

L542 000 828	External Cable Tally Punch
L542 000 829	External Cable Tally Reader
L542 000 826	External Cable Flexowriter

Part Number	Description	Type	Mfg.
	CONNECTORS		
339 188-3	36 Pin Amphenol Plug		
L520 009 013	34 Contact Socket Continental (Tally Reader-Punch)		
	MISCELLANEOUS		
339 265	Fan		
L200 011 853	Mounting Pad for	2N1183B	
339 270	Mounting Pad for other transistors		

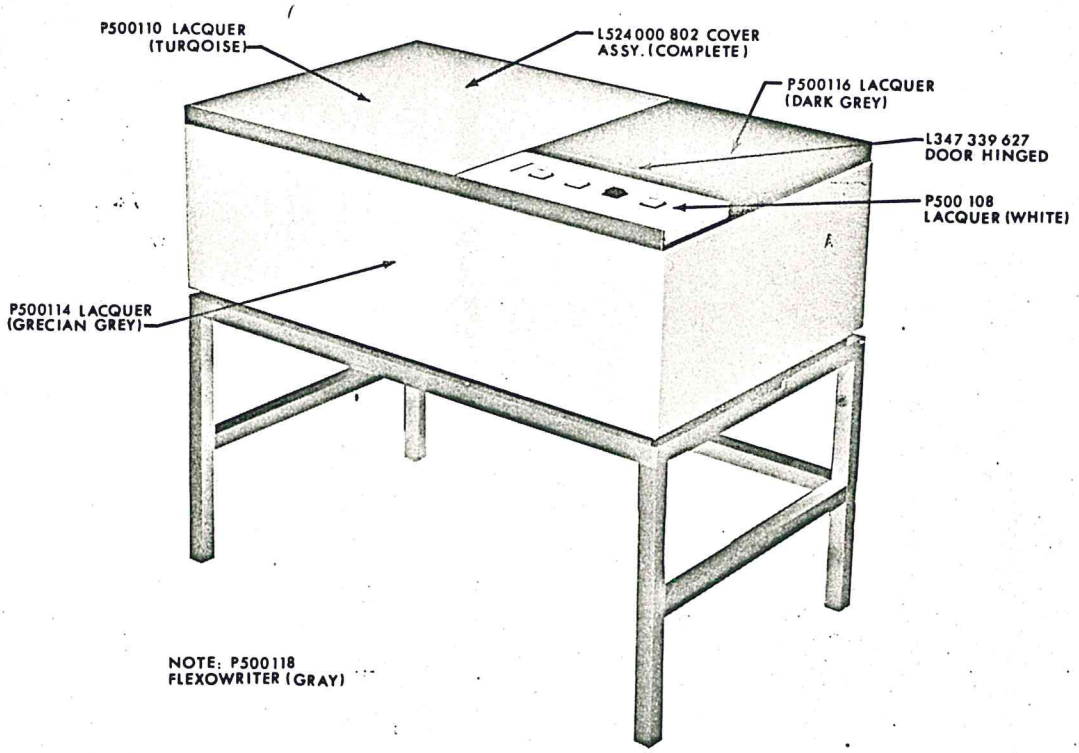


FIGURE 8-1 CONSOLE EXTERIOR FINISH

OSCILLOSCOPE DISPLAY UNIT PARTS LIST

CAPACITOR

L608 000 801	Capacitor, Variable	275 - 970 uuf, 250V
L605 009 023	Capacitor, Electrolytic	150uf, 350V
L605 000 740	Capacitor Tant.	6.8uf, ±10%, 35V
L605 009 001	Capacitor Ceramic	.005uf, 80%/-20
L605 000 684	Capacitor Tant.	10uf, ±10%, 20V
339 320-7	Capacitor Ceramic	1uf, ±20%, 25V
L605 001 693	Capacitor Ceramic	220pf
L605 009 027	Capacitor	.05uf, 3KV

RESISTOR

339316-80	Resistor	20K, 1/4W, ±5%
339316-53	Resistor	1.5K, 1/4W, ±5%
339316-9	Resistor	22 , 1/4W, ±5%
339316-62	Resistor	3.6K, 1/4W, ±5%
339316-66	Resistor	5.1K, 1/4W, ±5%
339316-70	Resistor	7.5K, 1/4W, ±5%
339317-36	Resistor	300 , 1/2W, ±5%
L603 000 820	Resistor, Variable	1 Meg, 2W, ±20%
L603 000 818	Resistor, Variable	250K, 2W, ±20%
L603 000 822	Resistor, Variable	25K, 2W, ±20%
L603 000 821	Resistor, Variable	5K, 2W, ±20%
339305-9	Resistor, Wirewound	2Ω, 2W, ±5%
339317-129	Resistor, Wirewound	2.2M, 1/2W, ±5%
339317-119	Resistor, Wirewound	820K, 1/2W, ±5%
339316-113	Resistor, Wirewound	470K, 1/4W, ±5%
339317-73	Resistor, Wirewound	10K, 1/2W, ±5%

TUBES

L530 000 801	Tube, 1V2
L530 000 043	Tube, 12AT7
L348 000 801	Tube, Cathode Ray, 5ABP1

FUSE

L505 000 821	Fuse, 1 Amp., 125V, SLO-BLO

Section 9

Model 101 Visual Oscilloscope Display

SECTION IX

MODEL 101 VISUAL OSCILLOSCOPE DISPLAY

9.1 GENERAL DESCRIPTION

The visual display unit, as used with the LGP-21 Computer System, sequentially displays the C, R, and A registers for a duration of one word time. The horizontal sweep and retrace time is one word period each, therefore, each of the three registers is displayed cyclically every 6th word time. Solid state gating and control circuits control the cyclic operation of the CRT sweep, through the horizontal and vertical output amplifiers.

The CRT is a 5" flat face RCA 5ABP1, with high deflection sensitivity. The electronic control circuits are as follows:

9.1.1 High Voltage Power Supply

The purpose of the high voltage power supply is to apply acceleration voltage to the CRT and a plate supply voltage for the horizontal and vertical output amplifiers. All other voltages are obtained from the computer.

9.1.2 Horizontal Deflection Generator

The horizontal deflection generator is basically a saw-tooth generator, which provides a linear signal (HO and $\overline{\text{HO}}$) to the grids of the horizontal output amplifiers. The inputs are E1 and T3d which provide an output sweep signal of two word times.

9.1.3 Horizontal Output Amplifier

The horizontal output amplifier takes the HO and $\overline{\text{HO}}$ outputs from the horizontal deflection generator as inputs to its grids and amplifies them as inputs to the CRT horizontal deflection plates.

9.1.4 Blanking Pulse Generator

The blanking pulse generator blanks out the sweep during retrace time for R and A. For the C display blanking is in effect during retrace and all bit times other than address time and sign time.

9.1.5 Word Time Counter

The word time counter is gated by T3 and defines trace and retrace time for each of the three registers, when the outputs are combined logically. It consists of a delay F/F for T3, three F/F's which have their outputs applied in such a way as to cause a cyclic output.

9.1.6 Vertical Input Gate

The vertical input gate takes the logical combinations of E2 and E3 gated with the C, R, and A register information to form output signal "Y" which applies the bit information to the vertical deflection generator.

9.1.7 Vertical Deflection Generator

The vertical deflection generator takes logical combinations of E2, $\overline{\text{E3}}$, E2 $\overline{\text{E3}}$ and Y input to form a tri-level stepping voltage with superimposed bit information. This signal (Ve, $\overline{\text{Ve}}$) is applied to the vertical output amplifier.

9.1.8 Vertical Output Amplifier

The vertical output amplifier uses the Ve and $\overline{\text{Ve}}$ outputs from the vertical deflection generator as inputs to its grids and amplifies them as inputs to the $\overline{\text{CRT}}$ vertical deflection plates.

9.1.9 Clock Pulse Amplifier

The clock pulse amplifier inverts cp to provide a positive clock to trigger the vertical input gate, blanking pulse generator and the T3d flip-flop.

9.1.10 Controls (External)

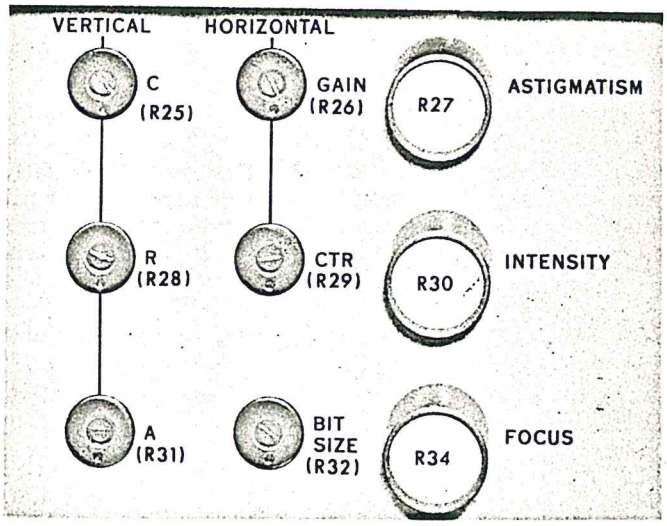


FIGURE 9-1 EXTERNAL CONTROLS

Focus (R34)	Potentiometer to vary the voltage on the CRT focusing grid.
Intensity (R30)	Potentiometer to adjust the cathode voltage on the CRT thus the acceleration beam brightness.
Vertical Position "C" (R25)	Controls the vertical position of the "C" Register trace.
Vertical Position "R" (R28)	Controls the vertical position of the "R" Register trace.
Vertical Position "A" (R31)	Controls the vertical position of the "A" Register trace.
Horizontal Center (R29)	Potentiometer to position the trace horizontally.
Horizontal Gain (R26)	Potentiometer to adjust the duration of the horizontal sweep sawtooth voltage.
Bit Size (R32)	Potentiometer to adjust the amplitude of the bits displayed.
Astigmatism (R27)	Potentiometer to adjust the voltage on the second anode of the CRT.

9.2 THEORY OF OPERATION

9.2.1 High Voltage Power Supply

The purpose of the high voltage power supply (Figure 9-9) is to provide sufficient acceleration to an electron beam to fluoresce the phospher coating on the face of the CRT. The acceleration voltage is achieved by full wave rectification of the high voltage secondary winding of the power transformer, by two 1V2 vaccum tube diodes with R-C network filtering. This provides a -1600 VDC potential to the cathode of the CRT (pin 2), through R30 a 250 KΩ intensity control, and +1600 VDC potential to the CRT anode.

A +300 VDC plate voltage supply is provided for the horizontal and vertical output amplifiers, by solid state rectification of the center tapped portion of the transformer secondary.

9.2.2 Horizontal Deflection Generator

The horizontal deflection generator (Figure 9-2) is a saw tooth generator with a two word time output pulse cycle. This output is used to control the horizontal sweep time of the CRT. The HO and $\overline{HO}$ output signals are applied directly to the control girds of the 12AT7 horizontal output amplifier.

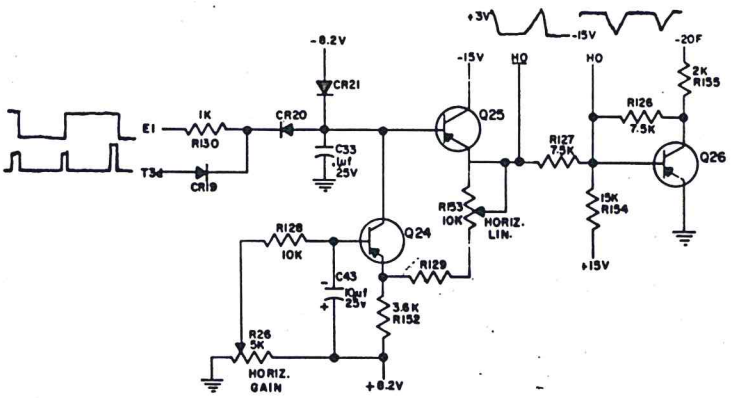


FIGURE 9-2 HORIZONTAL DEFLECTION GENERATOR

Assume that R26 and R153 are centered. Under these conditions the base of Q24 will be biased so that it will conduct, which will place a positive bias on the base of Q25, which will back bias CR21 and forward bias CR20.

When input E1 is true Q25 will be cut off since the base will be at approximately a +7.3 Volts and the emitter is at approximately +3 volts. When negative coincedance occurs between E1 and t3d, -20 volts will be applied to the cathode of CR21, which will forward bias it, applying -8.2 volts to C33 and the base of Q25. Q25 will then conduct causing the HO output to go from +3 volts to -15 volts and stay at -15 volts until t3d comes true. As t3d goes true CR21 will be back biased, and the negative charge on C33 will keep Q25 conducting during the RC discharge time of C33, the collector to emitter resistance of Q24, and R152. This will give a linear positive shift at output HO. The RC time is much longer than the word time, and the cycle will repeat before Q25 is cut off. Q26 is an inverter circuit which will follow the HO output, applying an equal signal to the other side of the output amplifier.

The horizontal linearity potentiometer (R153) controls the emitter voltage of Q24, and the positive base bias of Q25 which will effect the angle of discharge, thus linearity.

9.2.3 Horizontal Output Amplifier

The horizontal output amplifier (Figure 9-9) consists of a single 12AT7 dual triode amplifier. The saw tooth output of the horizontal deflection generator is applied directly to the control girds of the 12AT7. This amplified saw tooth is applied to the horizontal deflection plates of the CRT to pull the electron beam across the face of the CRT. By varying the horizontal center potentiometer R29, which is a current equalizing device, differences in conductivity, or amplitude of grid signals, can be compensated for. This allows the horizontal sweep to be centered on the face of the CRT.

9.2.4 Blanking Pulse Generator

The purpose of the blanking pulse generator (Figure 9-3), is to blank the CRT sweep during retrace time. The sweep for the three registers is blanked for the entire retrace period. The "C" sweep is also blanked during gating time for all bits except the sign bit and address bit time. This is to eliminate presenting the high order sector address.

This is accomplished by gating T3 S2 E2 E3 into Q8, so that Q8 will be cut off curing "C" gating time (E2 E3) at T3 and S2 time. With Q8 cut off -20 volts is applied to the base of Q9, causing it to conduct. As Q9 conducts 0 volts will be applied to the junction of C22 and CR9.

Assuming Q11 to be conducting and Q10 to be cut off, CR9 will be forward biased. The base of Q11 will be held at -.6 volt until CPM is applied. The base of Q11 will then go positive causing it to be cut off. Through normal flip-flop action Q10 will conduct. The 0 volt output of B1, from the collector of Q10, will therefore be applied to CR8 of the diode coupled gate.

The 0 volts applied to CR8 will be felt at the base of Q12, which will cut it off. This will apply -20 volts (B) to the control grid of the CRT. Thus the CRT will be blanked during the gating time of Q8 and during retrace time.

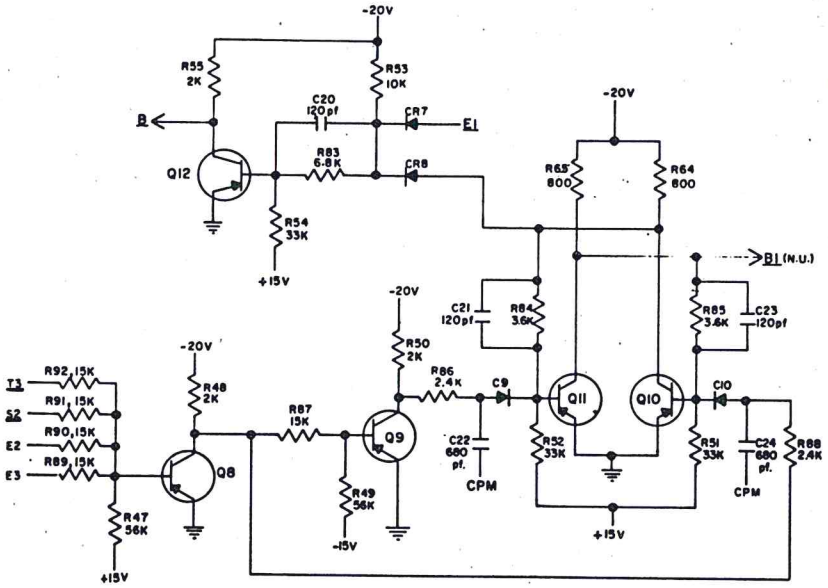


FIGURE 9-3 BLANKING PULSE GENERATOR

9.2.5 Clock Pulse Amplifier

The purpose of the clock pulse amplifier (Figure 9-4) is to invert the intermediate clock (Cp) to provide a positive clock (CPM) to time the display control circuits. Transistor Q31 is connected as an emitter follower and is biased to follow Cp. When Cp goes negative, Q31 will conduct applying approximately -13 volts at the base of Q30. This will cause Q30 to conduct, placing its emitter at essentially 0 volts. This 0 volts will be felt at the base of Q29, which is an NPN transistor, which will cause it to conduct. Q29's conduction path is from -15 volts, R110 emitter to collector, through CR13 which is now forward biased, to ground. As Q29 starts conducting, its emitter will swing from approximately -12 volts to 0 volts. C29 from the collector of Q29 to the base of Q30 is a speed up capacitor to keep the leading edge of CPM sharp.

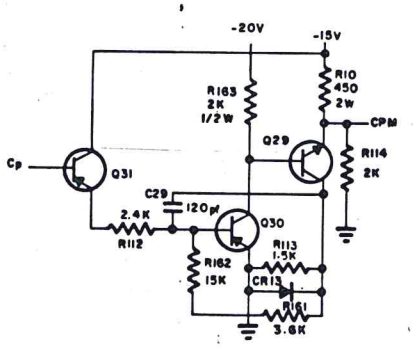


FIGURE 9-4 CLOCK PULSE AMPLIFIER

After 4.5μsec. as Cp goes positive, Q31 will cut off removing the negative bias to the base of Q30 cutting it off. When Q30 cuts off -20 volts is applied to the base of Q29, so it will stop conducting. This will back bias the cathode of CR13 to approximately +5 volts. Therefore CPM will be a positive going clock, from -12 volts to 0 volts.

9.2.6 Word Time Counter

The word time counter (Figure 9-11) is made up of three flip-flops (E1, E2, E3) which use the T3d flip-flip as an input toggle. The outputs E2 $\overline{E3}$ are added logically, and combinations of E2, $\overline{E2}$, E3, and $\overline{E3}$ are applied to the input gates of the horizontal and vertical control circuits, and the blanking pulse generator.

The E2 E3 outputs of the word time counter define "C" register sweep time; the E2 $\overline{E3}$ outputs define "R" register sweep time; and the $\overline{E2}$ $\overline{E3}$ outputs define "A" register sweep time. The E1 output which is one word time is gated to the horizontal control circuits to achieve a one word time sweep and retrace period for the CRT.

The T3d, E1, E2, and E3 flip-flops used in the word time counter are the same basic flip-flops that are in the computer. See Figure 3-2, page 3-3. The differences are the collector load resistor values and the collector to base feed back resistor values. Note that most flip-flops in the computer have a constant clock input which is capacitively coupled and wait on a steady DC gating level (4.5 μ sec. entrance time constant). However the flip-flops used in the word time counter differ in that their clock inputs are dependent on the positive rise of the DC levels applied to them. This uncommon clocking (in the case of the LGP-21 Computer) is noted in the logic as "d/dt" of $\overline{E1}$, E2, etc.

The following description will explain the operation of the word time counter, but will not go into a detailed explanation for each flip-flop.

The word time counter will count to "3" and reset itself, as seen in the following logic description. Reference will be made to the Timing Chart, Figure 9-14. Note that the sweep is for 6 word periods.

In order to display all bit information from the registers it is necessary to delay the CRT sweep by one bit time, so that T3 will be present on the sweep. The one bit delay is achieved through the T3d flip-flop.

T3d' - T3

The T3d flip-flop is gated by T3 and CPM, however coincidence occurs at the trailing edge of the T3 pulse, thereby delaying T3d by one bit time.

$\overline{T3d}'$ = T3d

E1' = $\overline{E1}$ d/dt$\overline{T3d}$

$\overline{E1}'$ = E1 d/dt$\overline{T3d}$

Since $\overline{T3d}$ is the clock input to the E1 flip-flop the word time counter is delayed one bit time. The E1 flip-flop will change state every word period, since it is gated by $\overline{T3d}$ and its own output.

E2' = d/dt$\overline{E1}$ $\overline{E2}$

$\overline{E2}'$ = d/dt$\overline{E1}$ E2 $\overline{E3}$

The E2' input is gated by E2 $\overline{E3}$ which is made up by modified NOR gate Q18. The output of Q18 is applied to the vertical deflection generator as the "R" gating signal, and to Q19. Q19's output is applied as the reset pulse to the E2 flip-flop. Since E2' = d/dt$\overline{E1}$ $\overline{E2}$ the E2 output will be true except during the 4th and 5th word periods, as seen on Timing Chart, Figure 9-14.

E3' = d/dtE2 $\overline{E3}$

$\overline{E3}'$ = d/dt$\overline{E1}$ E3

Since the outputs of the E3 flip-flop are connected to its opposite inputs, the E3 flip-flop will be controlled by the clock inputs d/dt→$\overline{E1}$ and dtE2. E3 will go true at the beginning of the sixth word period and stay true for two word periods, until the next positive $\overline{E1}$ output.

9.2.7 Vertical Input Gate

The vertical input gate (Figure 9-13) is made up of 5 NOR Gates and the "Y" flip-flop. This gate takes the bit information from the computer registers and at the proper time relationship applies it to the vertical deflection generator.

$Y' = E2\ E3\ C + E2\ \underline{E3}\ R + \underline{E2}\ \underline{E3}\ A$

In all cases the E2 and E3 configurations are the gating and retrace times for the respective registers.

9.2.8 Vertical Deflection Generator

The vertical deflection generator (Figure 9-11) is essentially a current summing device which applies different input impedances, for the three conditions of the word time counter, to define the sweep levels. These input impedances form three different base voltages for Q27, which are modified by feedback resistor R122. Thus the current summing inputs are applied to an amplifier rather than a switch as in the normal NOR gate configuration.

For the display of the registers, the voltage applied to the vertical output amplifier (Ve) is approximately -6, -7, and -8 volts dependent upon the level potentiometer adjustment, see Figure 9-5.

For the display of bit information the voltage applied to the vertical output amplifier (Ve) is between approximately -6 to -10 volts. The bit information will be superimposed on E2 and will follow the above voltage range, see Figure 9-6. The input impedances applied to the base of Q28 are modified by feedback resistor R118, therefore Q28 also acts like an amplifier to the input impedances. The approximate input and output waveforms are shown along with the voltage levels on the individual schematics.

9.2.9 Vertical Output Amplifier

The vertical output amplifier (Figure 9-9) consists of a single 12AT7 dual triode amplifier. R22 and R24 are current limiting resistors, and R23 is a current equalizing device. C8 and C10 are speed-up capacitors to assure that vertical linearity is maintained. C8 is adjustable to allow the necessary instantaneous bias levels during switching time.

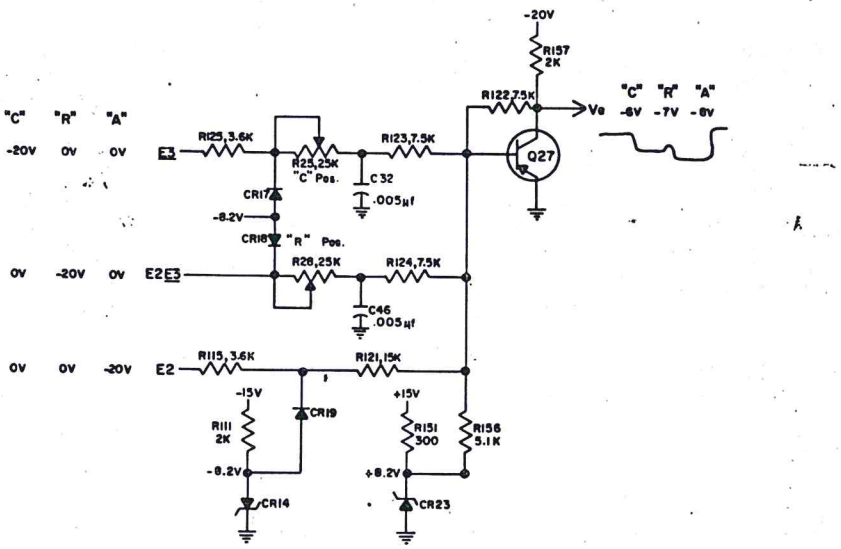


FIGURE 9-5 VERTICAL DEFLECTION GENERATOR - Ve OUTPUT

9.3 LOGIC EQUATIONS

$T3d' = T3$

$\underline{T3d'} = T3d$

$E1' = \underline{E1}\ d/dt\underline{T3d}$

$\underline{E1'} = E1\ d/dtT3d$

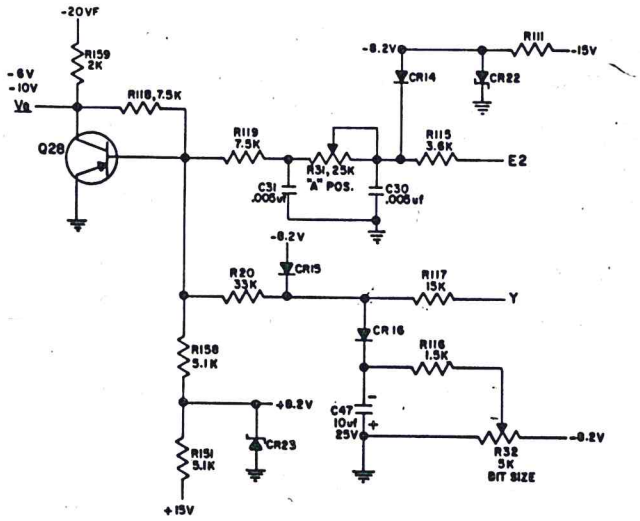


FIGURE 9-6 VERTICAL DEFLECTION GENERATOR - Ve OUTPUT

$E2' = \underline{E2}\ d/dt\underline{E1}$

$\underline{E2'} = E2\ \underline{E3}d/dtE1$

$E3' = \underline{E3}\ d/dtE2$

$\underline{E3'} = E3\ d/dt\underline{E1}$

$Y' = E2\ E3\ C + E2\ \underline{E3}\ R + \underline{E2}\ \underline{E3}\ A$

$B1' = E2\ E3\ \underline{S2}\ \underline{T3}$

$\underline{B1'} = \underline{E2} + \underline{E2} + S2 + T3$

$\underline{B1'} = E1 + \underline{B1}$

$CPM' = Cp$

9.3.1 Glossary of Logical Functions

T3d	Delay flip-flop which delays T3 one bit time.
E1	First flip-flop of the Word Time Counter.
E2	Second flip-flop of the Word Time Counter.
E3	Third flip-flop of the Word Time Counter.
Y	Flip-flop output of Vertical Input Gate.
B1	Flip-flop used as "C" blanking output.
B	Blanking pulse.
CPM	Inverted intermediate clock - positive clock.

A	Playback from the "A" register.
C	Playback from the "C" register.
R	Playback from the "R" register.
T3	Inverted sign term.
Cp	Intermediate clock.
S2	All bit times except address time.

Section 10

Data Input / Output

SECTION X

DATA INPUT/OUTPUT

10.0 INTRODUCTION

To expand the capabilities of the LGP-21 computer, a card called the "Data Input-Output Card" was developed. It will allow use of the LGP-21 system with input-output devices not included in the basic system.

This card is designed to control the transfer of data between the computer accumulator and its input-output terminals. Control and response lines are provided to facilitate transfer of data whether the external device is faster and must be controlled by the computer or slower and must furnish control signals to the computer.

Data is transferred in 4 or 6 bit parallel characters in groups of 8 or 5 respectively, dependent on the command being executed.

10.1 TERMINOLOGY

The following is a list of logical terminology used on the Data I/O Board.

Ad	Select Code Gate
$\overline{\text{Cd}}$	Not Code Delete
CNR	Character Not Ready
CRY	Character Ready Signal
D1-D2-D3	Input Character Counter
$\overline{\text{Faf}}$	Input-Output Interlock
$\overline{\text{Fc}}$	Set Term for the F Flip-Flop
$\overline{\text{Fd}}$	Reset Term for F Flip-Flop
F I/O	Selection Flip-Flop
F I/Om	Word Ready Signal
$\overline{\text{Ga}}$	Inhibit Term for "ON" side of "G" Flip-Flop
$\overline{\text{Gc}}$	Set Term for "G" Flip-Flop
IN-1 thru IN-6	Input lines from external devices
$\overline{\text{IN-1}}$ thru $\overline{\text{IN-6}}$	Input lines from external devices
$\overline{\text{Lc}}$	Last character signal
$\overline{\text{Lo}}$	Output load signal. (Causes a clock pulse to set output storage F/F's)
Lp	Step signal
OC	Output Clock
OC+	Inverted $\overline{\text{OC}}$
OR*	Output device ready
ONR	Output device not ready
01-06	Data output lines
$\overline{\text{01}}$-$\overline{\text{06}}$	Data output lines
011-066	Output lines from output data storage flip-flops
$\overline{\text{011}}$-$\overline{\text{066}}$	Output lines from output data storage flip-flops

P1c-P6c P1d-P6d	Set terms formed to set "P" flip-flops during I order Reset terms to reset "P" flip-flops during I order
Q2c	Set term for Q2
Sc	Not a stop code
Scs	Inhibit Ø4 on control character. code delete, and stop code when device selected and ready.
Sk	Not a control character

10.2 COMPLETE LOGIC EQUATIONS

Ad = (FG P2 P3 P4 P5 Q3 Q4 be Faf) (P1 + P1)

Ø3 Device; 5400 I or 2200 (Dec.) 30; or P; Not execute button; No device Selected

Cd = P1 + P2 + P3 + P4 + P5 + P6

cd = P1 P2 P3 P4 P5 P6

NR = External Signal
CRY = External Signal

D1' = D2
D1' = D2
D2' = D3
D2' = D3
D3' = G
D3' = G

Faf = F I/O

Fc = F' = F G T3 F I/O CRY Sc Q3

F I/O' = (F I/Om Ad Q2 T3 Q1) + (T3 Q2 Ad Q1)

F I/O' = Scs FG T3 F I/O OR LC + F G Q3 T3 Sc + Lo + To

Gc = Scs F G T3 OR F I/O Lc

Q2c = Scs F G T3 OR F I/O Lc

o = F G T3 Q3 OR F I/O ONR

Lp = F G S2 F I/O

OC' = Lo
OC' = Lo

01 = 011
01 = 011
02 = 022
02 = 022
03 = 033
03 = 033
04 = 044
04 = 044
05 = 055
05 = 055
06 = 066
06 = 066

011' = P1
$\overline{011'}$ = $\overline{P1}$
$\overline{022'}$ = $\overline{P2}$
022' = P2
$\overline{033'}$ = $\overline{P3}$
033' = P3
$\overline{044'}$ = $\overline{P4}$
044' = P4
$\overline{055'}$ = $\overline{P5}$
055' = P5
$\overline{066'}$ = $\overline{P6}$
066' = P6

OR' = OR* Q3 + $\overline{CNR}$ $\overline{Q3}$
$\overline{OR'}$ = S2

ONR' = External Signal
$\overline{ONR'}$ = $\overline{F\ I/O'}$

P1c = Lp IN -1
P1d = Lp $\overline{IN\ -1}$
P2c = Lp $\overline{IN\ -2}$
P2d = Lp $\overline{IN\ -2}$
P3c = Lp $\overline{IN\ -3}$
P3d = Lp $\overline{IN\ -3}$
P4c = Lp $\overline{IN\ -4}$
P4d = Lp $\overline{IN\ -4}$
P5c = Lp $\overline{IN\ -5}$
P5d = Lp $\overline{IN\ -5}$
P6c = Lp $\overline{IN\ -6}$
P6d = Lp $\overline{IN\ -6}$

Sc = P1 $\overline{P2}$ $\overline{P3}$ $\overline{P4}$ $\overline{P5}$ $\overline{P6}$
Cd = P1 $\overline{P2}$ $\overline{P3}$ $\overline{P4}$ $\overline{P5}$ $\overline{P6}$
SK = K $\overline{P5}$ $\overline{P6}$

Scs = F $\overline{G}$ T3 F I/O OR (SK + Cd + Sc)

10.3 THEORY OF OPERATION

The data input-output board is a control device to allow input of data to the computer and output from the computer, utilizing external input-output devices which are not manufactured specifically as a component device for the LGP-21 system.

All data transmission is in the form of 4 or 6 bit parallel characters. Four or 6 bit mode is determined by computer command.

All data lines require a signal voltage level of either zero volts _ one volt (true) or minus twelve to minus twenty volts (false) input impedance is at least 5000 ohms and the output source impedance is approximately 800 ohms.

10.3.1 Device Selection

The selection of a device at sign time of the first phase three of an input order or phase three sign time of a print order to make Faf come true is a coincidence between the signal Ad and the Q settings for either an input order or a print order to turn the F I/O flip-flop on.

F I/O' = Q1 $\overline{Q2}$ Ad T3 $\overline{Q1}$ Q2 Ad $\overline{F\ I/Om}$ T3

Print Address Order — Input Address Order

Ad = F $\overline{G}$ $\overline{Q3}$ $\overline{Q4}$ P2 $\overline{P3}$ P4 P5 $\overline{Faf\ be}$ (P1 $\overline{P1}$)

Ø3 P or I — 2700 or 1100

10.3.1.1 Input

Assuming an input device has been selected and the computer is sitting in blocked state phase one waiting for a character to be presented, the computer will input a character by going to phase three and setting the "P" flip-flops from the data input lines (IN-1 through IN-6). However, the character ready signal (CRY), which corresponds to P* from the flexowriter must be true to allow Fc to come true to force phase 3.

Ø1 Signtime

Fc = $\underline{F}$ $\underline{G}$ T3 $\underline{Q3}$ $\underline{Sc}$ CRY F I/O

Not output
Not Stop Code
Character Ready Signal
Device Selected

When phase three is entered, the signal Lp come true during address time (approximately 150μ secs.) allowing the "P" flip-flops to be set according to the states of the six data input lines.

P1' = P1c = Lp IN-1
$\underline{P1'}$ = P1d = Lp $\underline{IN-1}$
$\overline{P2'}$ = P2c = LP $\overline{IN-2}$
etc.

After Lp goes false the input device must drive the "character ready" (CRY) line false and the "character not ready" (CNR) line true for at least one millisecond. This causes the "OR" flip-flop to be turned on to allow Gc to come true which causes the computer to enter phase four and shift the P's into the accumulator.

Gc = $\underline{G}$ T3	OR	$\underline{Sc}$	$\underline{Cd}$	$\underline{Sk}$	$\underline{Lc}$	F I/O
Phase 3 signtime	Character not ready	not stop code	not code delete	not control character	not last character	device selected

The input device must then present the next character and set the "character ready" (CRY) line true. "OR" will be turned off by S2 when CNR goes false. If a control character, or a code delete is sensed Scs will go to -20V, making Fd go true and inhibiting phase four for that operation. If a stop code is sensed in phase three, Sc goes to -20V inhibiting phase four and turning the select flip-flop off.

Scs = F $\underline{G}$ T3 F I/O OR (SK + Cd + Sc)

$\underline{Fd}$ = $\underline{Scs}$

$\underline{F\ I/O}'$ = $\underline{F}$ $\underline{G}$ T3 $\underline{Q3}$ Sc + . . .

If the input device is capable of driving the character ready (CRY) line false less than 1 MS after Lp comes true, it should not be connected to the "character not ready" (CNR) line as this will exceed the maximum input rate of one character per 1.2 MS.

The data I/O card contains a binary counter (D1, D2, D3), which is reset when the selection flip-flop is turned on.

F I/O' = Q1 Q2 Ad T3 + $\underline{Q1}$ Q2 Ad F I/Om T3
RST = F I/O'

During the operation of the input order when "G" goes false at the end of phase 4 after entering the character, the counter is advanced by one.

$$D1' = D2$$
$$\underline{D1}' = \underline{D2}$$
$$D2' = D3$$
$$\underline{D2}' = \underline{D3}$$
$$D3' = G$$
$$\underline{D3}' = \underline{G}$$

The state of the counter is constantly available to the input device through six control signal lines. The input device may decode these lines and apply a false signal on the "last character" (LC) line when the counter indicates either 5 or 8 characters have been entered depending on whether the computer is in 4 or 6 bit mode.

If the input device is incapable of terminating the input order in either of the previously discussed ways, a constant may be used to initialize the accumulator by program so that on the 4th or 7th character shifted into the accumulator, the constant will be shifted into the "P" flip-flops as a stop code configuration. The stop code configuration of the flip-flops being present in phase one of the input order will terminate the input order by turning the F I/O flip-flop off.

This will make Faf true and allow a normal phase one to occur.

Characters are input at a rate up to one per 1.2 MS, limited by the speed of the input device.

A group of characters may be input and stored at a maximum rate of one group per 14 MS if the number of characters is one to five. If there are 6 to 8 characters per group, the maximum rate is one per 64 MS.

10.3.1.2 Output

Device selection for the execution of a print order is essentially identical to device selection for an input order in that the signal Ad, which defines the device select code address is applied to a gate which defines the print order.

$$Ad = (F\ \underline{G}\ P2\ \underline{P3}\ P4\ P5\ \underline{Q3}\ \underline{Q4}\ \underline{be}\ \underline{Faf})\ \ (P1 + \underline{P1})$$

$$F\ I/O' = Q1\ \underline{Q2}\ T3\ Ad + \ldots$$

This occurs at signtime of phase three. During phase four the P flip-flops are set to the confiruga-tion of the last six bits of the A register. At signtime of phase four Q3 is turned on to indicate an output or print order. This allows the "output device ready" (OR) signal to come true, if the external device has signaled that it is ready to accept output from the computer. This is done by driving the OR* line true.

$$OR' = OR^*\ Q3$$

The "output not ready" flip-flop (ONR) has an entrance time constant of 15 microseconds, therefore, the external signal (ONR') supplied by an external output device must be true for at least 15 microseconds. OR and ORN being true allow Lo (output load) signal to go false.

$$Lo = \underline{F}\ \underline{G}\ T3\ Q3\ F\ I/O\ OR\ ONR$$

This makes OC' come true to form the output clock OC. OC coming true sets the output buffer flip-flops 011-066 to the same configuration as the "P" flip-flops.

$$011' = P1\ OC$$
$$\underline{011}' = \underline{P1}\ OC$$
etc.

The positive going signal from S2 turns the "OR" flip-flop off preventing another OC until the next execution of a print order. When Lo goes false at sign time of phase one, the F I/O selection flip-flop is turned off, terminating the print mode.

$$\underline{F\ I/O}' = Lo + \ldots$$

The output not ready line is driven false by

$$\overline{ONR'} = \overline{F\ I/O'}$$

Characters can be output from the computer at rates up to one per 14 milliseconds.

10.4 WIRING DIAGRAMS AND SCHEMATICS

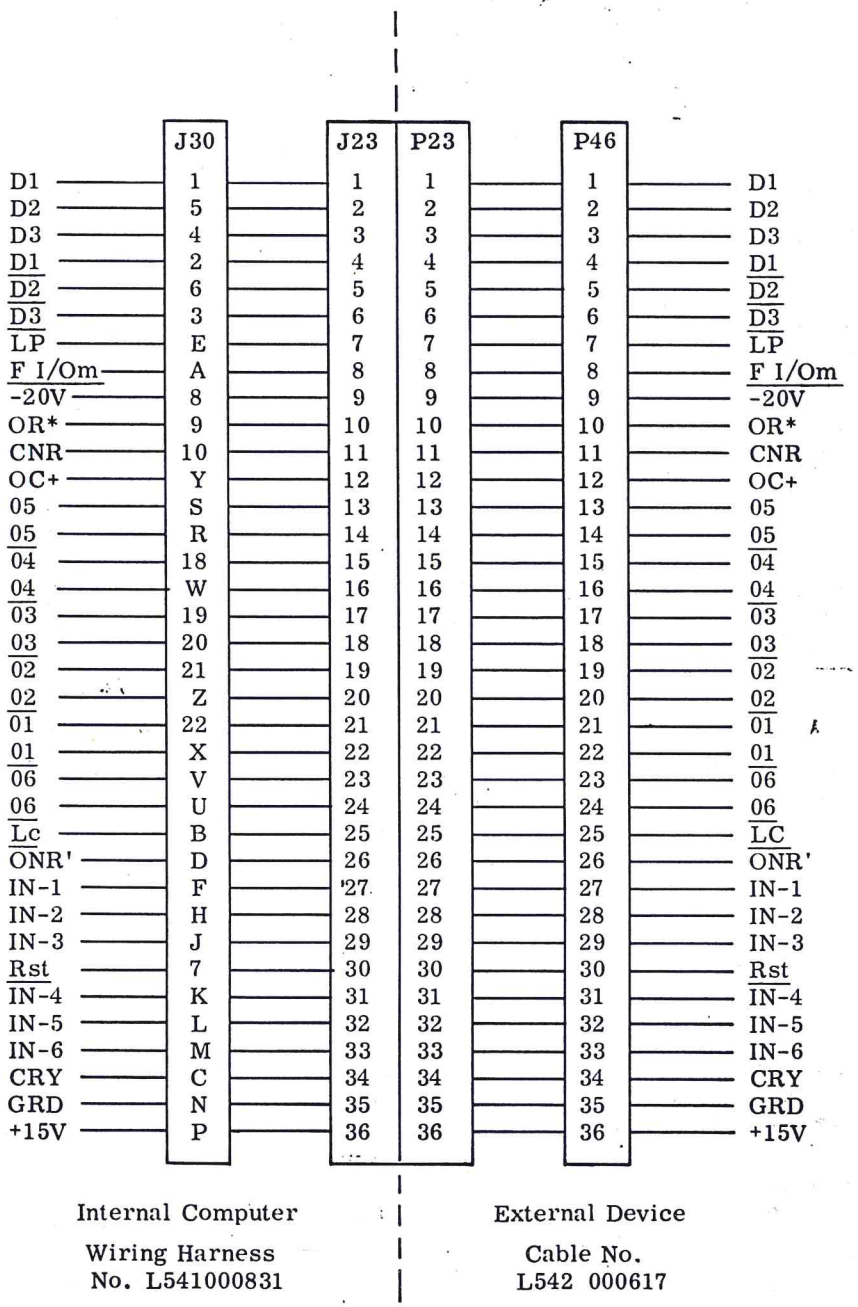
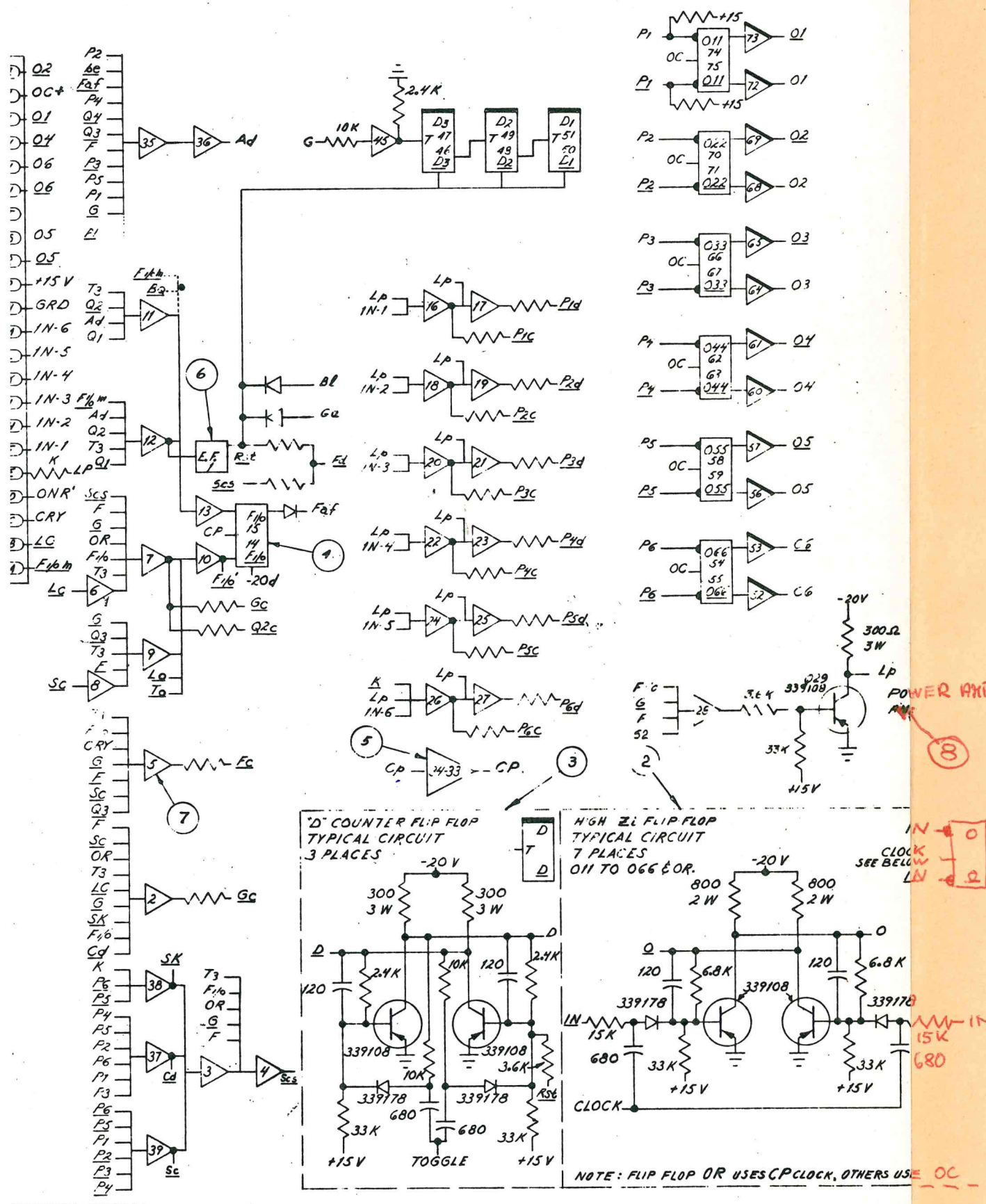
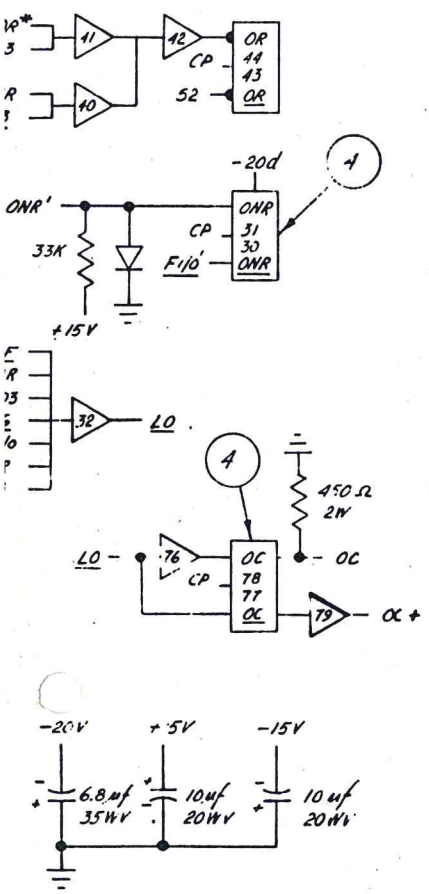
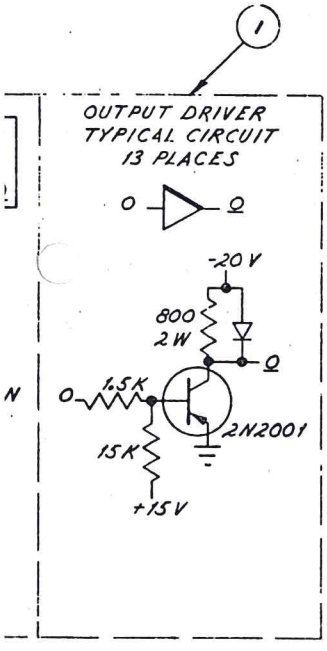


FIGURE 10-1 CABLE DIAGRAM (INTERNAL DATA I/O TO EXTERNAL I/O DEVICE



UNLESS NOTED:
RESISTORS ARE 15K, ¼ W, ±5%
K FOR BL ON Q13 OF PHASE CONTROL.
5Ω FOR Q2C ON PEQ CARD
HARNESS SEE L541 000 831.





REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

ITEM NO.	QTY REQD	PART OR IDENTIFYING NO.	MATERIAL SIZE, DESCRIPTION & SPECIFICATION
8	1	——	POWER AMPLIFIER
7	35	L543 338 428	NOR GATE
6	1	L543 338 433	EMITTER FOLLOWER
5	1	L543 338 434	CLOCK DRIVER
4	3	L543 338 431	FLIP FLOP (F/lo & ONR FF's HAVE 800Ω COLLECTOR RESISTORS)
3	3	---- ----	"D" COUNTER FLIP FLOP TYPICAL CIRCUIT
2	7	——	HIGH ZL FLIP FLOP TYPICAL CIRCUIT
1	13	——	OUTPUT DRIVER, TYPICAL CIRCUIT

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON DIMENSIONS
DECIMAL ANGULAR
2 PLACE ±.02 ±1°
3 PLACE ±.010
4 PLACE ±.0005
MATERIAL
FINISH

DRAWING GRADE
DR 28 MAR 63
CHK 1 MAY 63
ENGR 1 MAY 63
APPD 22 MAY 63
ISSUED BY

N/A L535 004 673

LIBRASCOPE GENERAL PRECISION
LIBRASCOPE DIVISION · GENERAL PRECISION, INC., GLENDALE 1, CALIFORNIA

LOGIC DIAGRAM
DATA I/O
LGP-21 COMPUTER

CODE IDENT NO. 36090 | SIZE D | L200 014 653
SCALE —— | SHEET

L200 014 653

FIGURE 10-2 LOGIC DIAGRAM DATA I/O CARD

LGP-21 COMPUTER SYSTEM REFERENCE MANUAL

Preliminary Version

This manual is intended as a basic introduction to the LGP-21 computer system. It summarizes all LGP-21 hardware features, operating procedures and programming techniques. A more complete treatment of these topics will be found in the LGP-21 programming manual.

LGP-21 COMPUTER SYSTEM

PROGRAM AND DATA MANIPULATION

TABLE I

TABLE II

TABLE III

ILLUSTRATIONS

GENERAL CHARACTERISTICS

The LGP-21 is a compact digital computer with a large, 4096-word memory. It is completely mobile, can be plugged into any convenient outlet, and is fully transistorized for reliable operation and ease of maintenance.

This computer was designed as an economical solution for the general purpose computation needs of business, engineering and science. Operation and programming can be learned within a few days, even by personnel with no previous knowledge of computers. A compact vocabulary of 23 instructions is easily mastered and allows simple programming of complex problems.

The basic LGP-21 System includes the Model 21 Computer and the Model 121 Tape Typewriter input/output unit. For users who require greater input/output speeds, the following auxiliary equipment is also available: the Model 141 Paper-Tape Reader and the Model 151 Paper-Tape Punch, which process information at 60 characters-per-second.

Another auxiliary device for the LGP-21 is the Model 101 Visual Oscilloscope Display which provides a visual representation of the three LGP-21 control registers. This is useful in locating errors during program checkout, and in providing a visual indication of the key locations at which a program may stop during operation.

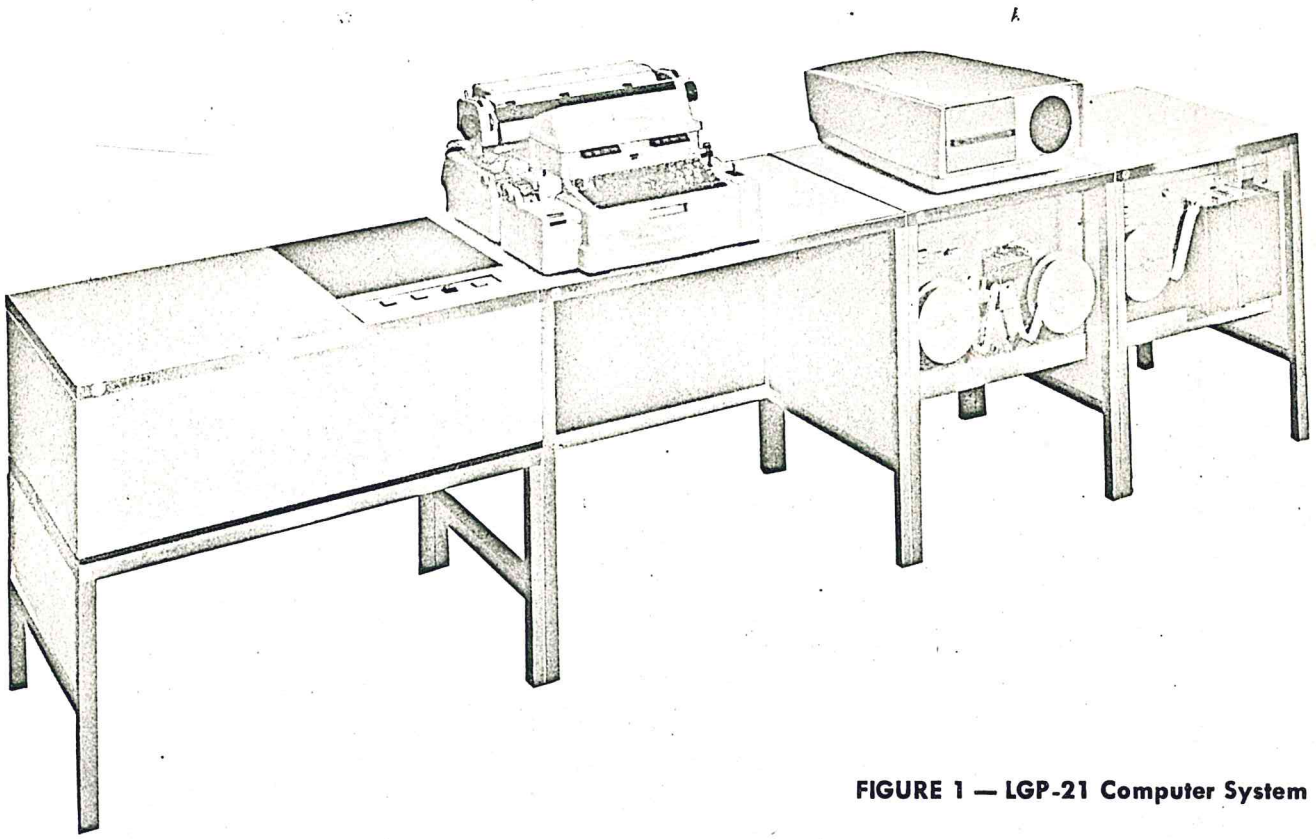


FIGURE 1 — LGP-21 Computer System

Input/Output Device

The LGP-21 System will accommodate up to 32 input and output devices in any desired combination. They are selected individually under program control. Output operations can be performed on more than one device.

The primary input/output device for the LGP-21 is the Model 121 Tape Typewriter. This device has a standard alphanumeric keyboard, a paper-tape reader, a paper-tape punch, and special control levers.

Information can be input automatically from the tape reader to the typewriter and then to the computer at 10 characters-per-second, or manually from the typewriter keyboard to the computer. Output information from the LGP-21 can be recorded by the typewriter or by the typewriter and tape punch at 10 characters-per-second. Input and output data is normally in decimal notation, while internal computation is performed in binary by the LGP-21. Conversion to binary, for this purpose, is achieved automatically through programming.

Word Structure

The LGP-21 processes all information as 32-bit words ("bit" is derived from "binary digit"). Each word consists of a sign bit, 30 bits of information, and a spacer bit. When dealing with binary values, the presence of a bit value is indicated by "1", the absence by "0". The sign bit contains a 1 to represent a negative word, or a 0 to represent a positive word. The spacer bit is used to separate adjacent words on the memory disc and is always recorded as 0.

The binary configuration of the 32 bits may represent either a numerical value (data word) or a computer instruction (instruction word). Data and instructions may be intermixed in memory, and the same unit of information can be used as data or instruction at different points in a program.

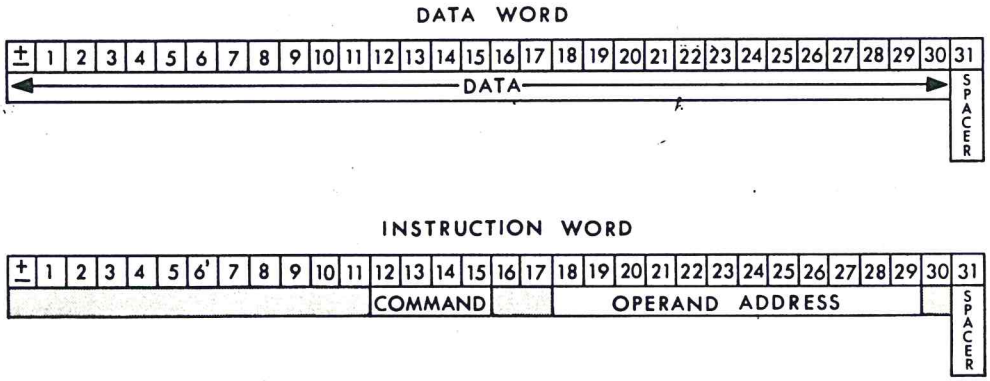


FIGURE 2 — Word Structure

When a word is used for data, the numbers are normally held in binary notation. The 30 significant binary digits in an LGP-21 word can represent decimal values up to 1, 073, 741, 823. Decimal numbers can also be represented by a system of notation called binary-coded decimal. As many as eight decimal digits, representing any positive number less than 80, 000, 000, can be held in a binary-coded decimal word. Various capabilities for negative numbers and fractions can be deduced. In place of a numerical value, a word may contain up to five alphanumeric characters. Two or more binary or decimal numbers can be packed into the same word as long as their combined requirements do not exceed 30 bits plus sign.

When a word is used to represent an instruction, it contains one basic command (bits 12 through 15) and an operand address (bits 18 through 29). The remaining bits are available—except for the sign bit which is significant in the case of

certain commands—and do not affect the instruction. The command determines what type of operation is to be performed, i.e., addition, subtraction, division, etc. The operand address for most instructions identifies the location within memory of the quantities related to the operation. For transfer instructions it will contain the address of the next instruction to be executed in the event of an active transfer.

MEMORY

Information is recorded in the form of magnetized spots on the surface of a rotating disc. When the disc is idle, the read/write heads rest on its surface; but when the disc attains operating speed, air pressure causes the heads to float at the correct operating position. The memory disc revolves at 1180 rpm. Thus, one revolution requires about 52 milliseconds. One word-time—the time required for one word to pass under a read head—is therefore about 0.40 millisecond.

Figure 3 illustrates the relationship of the sectors to their respective read/write heads.

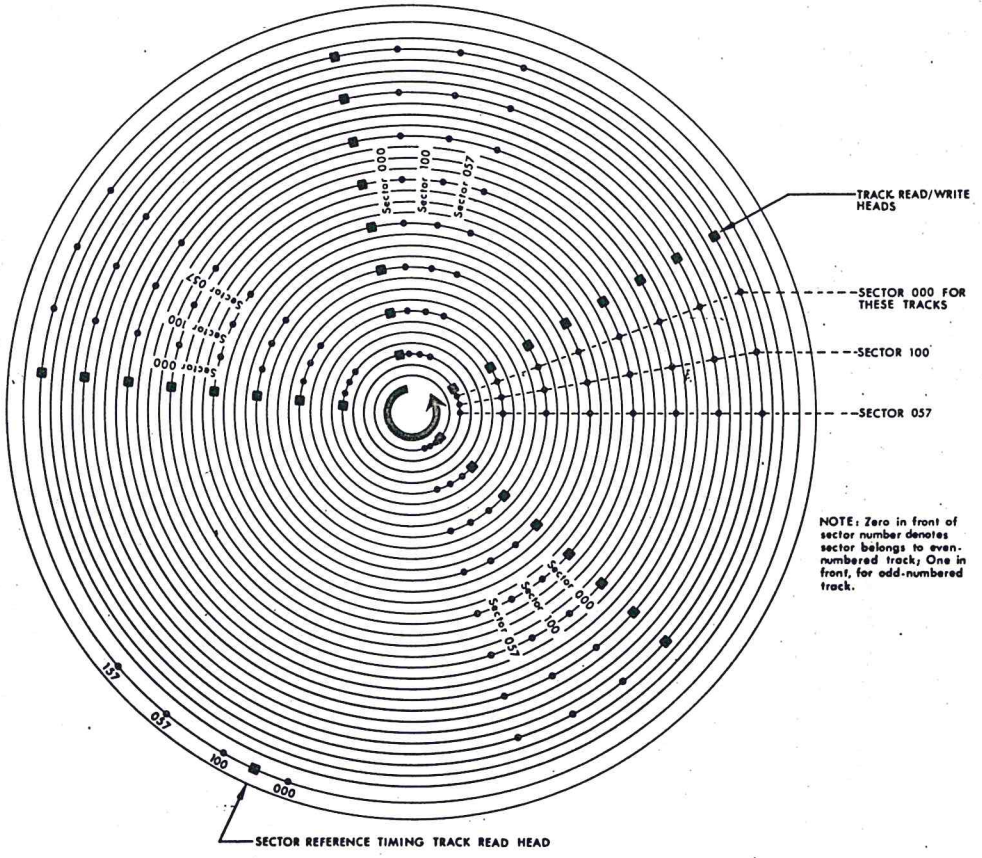


FIGURE 3 — Memory Disc

The memory disc has a total capacity of 4096 words or sectors. The sectors are divided into logical groups of 64 called tracks. There are a total of 64 tracks in memory. Both tracks and sectors are numbered 00 through 63. The location of any word in memory can be specified by its track and sector number. This number is known as the address of the word. For example, 2347 is the address of the word in Track 23, Sector 47. Consecutive addresses are 0000, 0001, 0002...0063, 0100...6361, 6362, 6363, 0000.

Mounted above the surface of the memory disc are 32 read/write heads which inscribe concentric circles as the disc revolves. Each read/write head serves two tracks, which are assigned alternate sectors in a circle. Thus read/write head number 1 reads the first sector of track 00, then the first sector of track 01, second sector of track 00, second sector of 01, and so on.

The sectors are not numbered sequentially within the tracks, but the pattern of the numbering is the same for all. It is based on an 18-word interlace which positions consecutive words 18 sectors apart and provides a 7.26 ms timing interval between them. This permits the optimizing of operand addresses for instructions which are executed in sequence.

COMPUTER CONTROL

All computer functions are controlled by three registers and their associated circuitry which comprise the arithmetic and computing control elements. The three control registers are designated: Accumulator (A), Instruction Register (R), and Counter Register (C). These registers are recirculating lines in a single track on the memory disc. A recirculating line has a read-head and a write-head, located 1 word-time apart, which continually copies information from one sector into another. Thus, the same word is available at every word-time.

A fourth register on the same track is the Extended Accumulator. Its read-head and write-head are located 2 word-times apart. This register records the double-length product of the multiply operation. Depending upon the command used, the most or least significant half of the double-length product is recorded in the normal Accumulator. This half can be stored in memory for future use.

Figure 4 shows the relationship of the registers on the recirculating line.

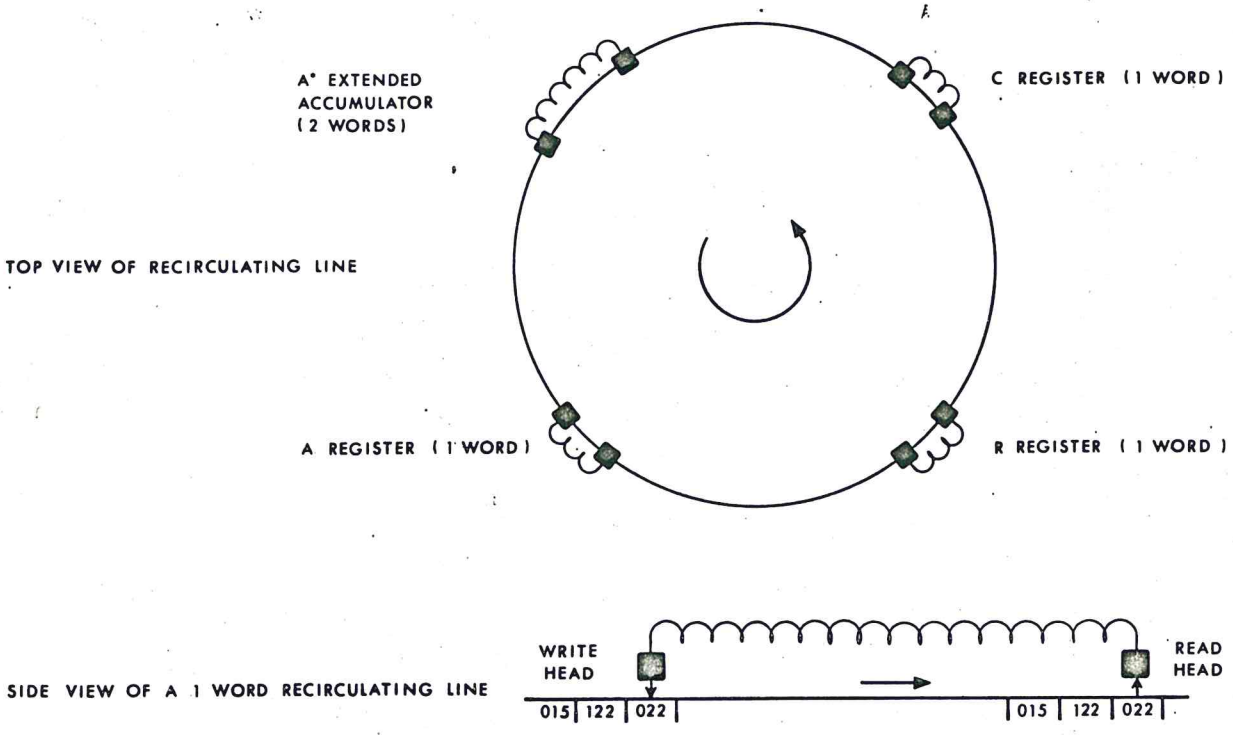


FIGURE 4 — Control Registers

Accumulator

The Accumulator, register A, is the working register used for all manipulation of data. It is the register through which all information passes between the computer and its input/output devices, as well as from one part of memory to another.

The Accumulator contains one of the operands prior to execution of an arithmetic instruction and the result of the arithmetic operation after execution. The second operand is a word in memory whose location is specified by the address portion of the instruction. The structure of the Accumulator is the same as that of a memory word (a sign and 31 bits), except that the spacer bit in the Accumulator can contain a 0 or 1 as the result of input. A multiply operation develops a double-length product (62 bits), either half of which can be retained in the Accumulator.

Instruction Register

The Instruction Register, R, holds the instruction being executed by the computer. Instructions in the stored program are transferred one at a time in sequence to the Instruction Register for execution. The contents of this register specifies the operation to be performed and the word in memory with which or upon which to operate. The configuration of the Instruction Register is the same as that of an instruction word.

During multiply and divide operations, the Instruction Register contains the multiplier or divisor rather than the instruction.

Counter Register

The Counter Register, C, contains the address of the next instruction to be executed. After executing an instruction, the computer searches for the word whose address is in the Counter. That word is transferred to the Instruction Register to be executed, and the contents of the Counter are incremented by 1. There are two commands (T and U) which set the Counter Register to a specified address.

If overflow occurs—that is, if a quantity beyond the capacity of the Accumulator has been generated—due to the execution of an add, subtract, or divide instruction, a 1 is recorded in the sign position of the Counter Register. The overflow bit may be examined and reset to 0 by a negative Sense and Transfer instruction, for example, 800Z0200.

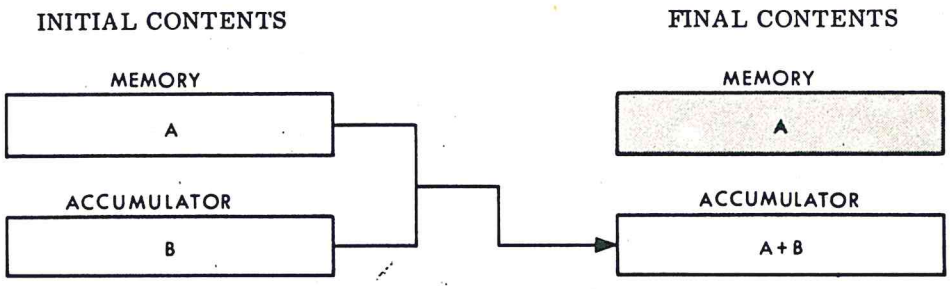
COMMAND LIST

The Command List

The LGP-21 has a repertoire of 23 commands. An instruction is a combination of a command and an operand address. Each instruction commands the computer to perform one of its built-in operations. The following list shows the commands and the effect of each. When the address is shown as "m", any memory location could be designated as the operand of that instruction. When the address is shown as "t", the track number is significant as a code, while the sector number is irrelevant and does not affect any function of the instruction.

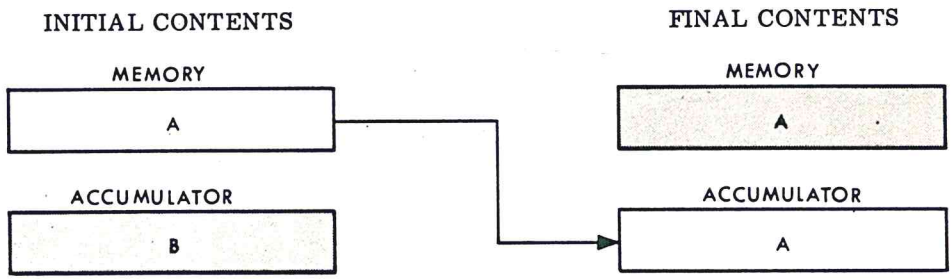
Am ADD

Add the contents of location m to the contents of the Accumulator; the sum replaces the contents of the Accumulator. If an addition results in a number that is outside the limits of the Accumulator, overflow will occur. Memory remains unaltered.



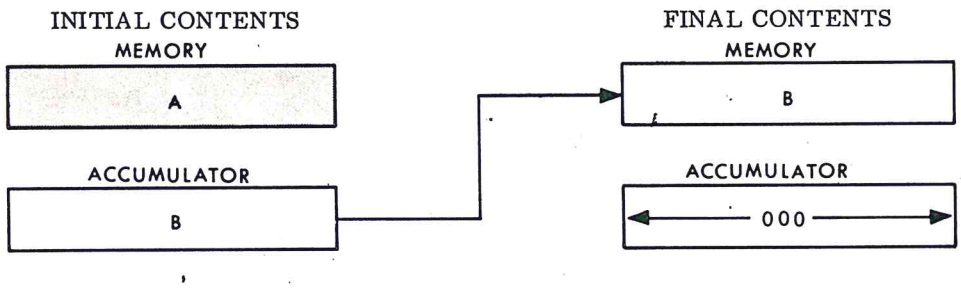
Bm BRING

Bring the contents of location m to the Accumulator, replacing its contents. Memory remains unchanged.



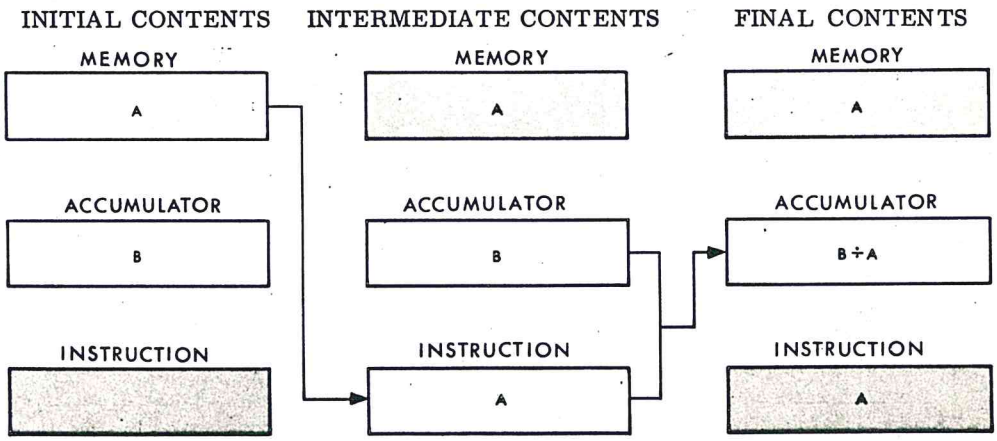
Cm CLEAR

Store the contents of the Accumulator in memory location m; then clear the Accumulator to zero.



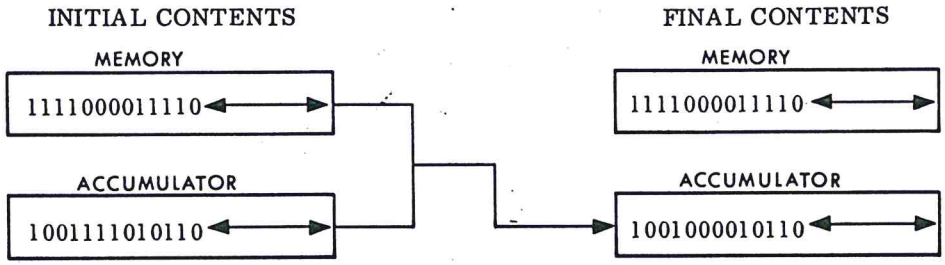
Dm DIVIDE

Divide the number in the Accumulator by the number in location m, retaining the quotient, rounded to 30 bits, in the Accumulator. The absolute value of the contents of m must be greater than the absolute value of the contents of the Accumulator, or overflow will occur. During the divide operation, the Instruction Register holds the divisor.



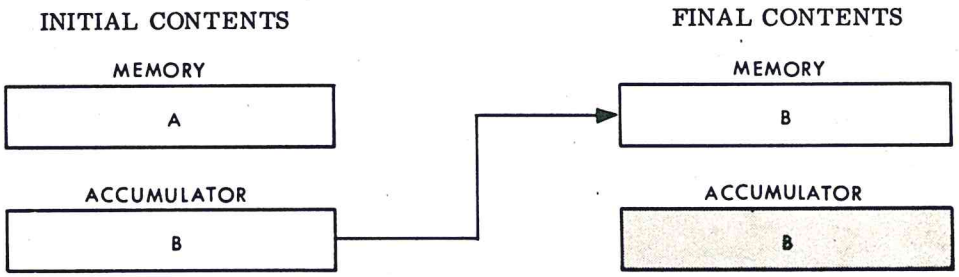
Em EXTRACT

Where "1" bits are in location m, retain the value of the corresponding bit positions in the Accumulator; where "0" bits are in m, place 0 bits in the corresponding positions in the Accumulator. The word in m is called the "mask" and remains unaltered.



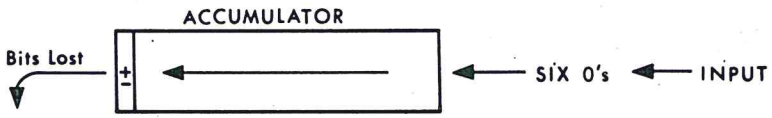
Hm HOLD

Store the contents of the Accumulator in location m, without altering the contents of the Accumulator.



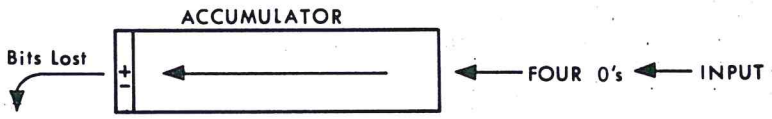
It INPUT 6-BIT

Shift the contents of the Accumulator left 6 bits, inserting zeros at the right; then give a start read signal, allowing the 6 bits of each character read by the input device specified by t to enter the Accumulator. (See Input Note below.)



-It INPUT 4-Bit

Shift the contents of the Accumulator left 4 bits, inserting zeros at the right; then give a start read signal, allowing 4 bits of each character read by the input device specified by t to enter the Accumulator. (See Input Note below.)



Input Note: Input is terminated when a stop code is read following the least significant character. The Model 141 Paper-Tape Reader can also enter fixed word-length items by any method of programming that leaves the binary configuration of a stop code in a particular position in the Accumulator to delimit the word length. When the 4-bit (1000) or 6-bit (100000) configuration of a stop code is pushed past bit position zero of the Accumulator, input will be stopped.

The fixed word-length mode of input cannot be used with the typewriter since it needs to read a stop code to halt its reader. The 141 Paper-Tape Reader will

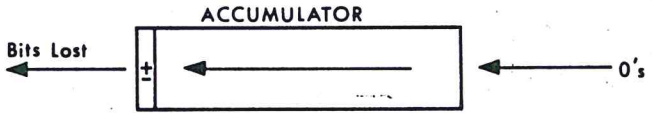
cease input when a stop code is read or when a stop code is pushed out the Accumulator on the left, whichever occurs first.

The following table shows hexadecimal constants that will position a stop code to delimit the word length.

Number of Characters	4-Bit Input	6-Bit Input
1	08000000	02000000
2	00800000	00080000
3	00080000	00002000
4	00008000	00000080
5	00000800	00000002
6	00000080	--------
7	00000008	--------

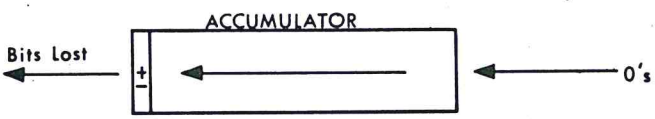
It SHIFT 6-Bits

When t = 62, shift the contents of the Accumulator left 6 bits, inserting zeros at the right.



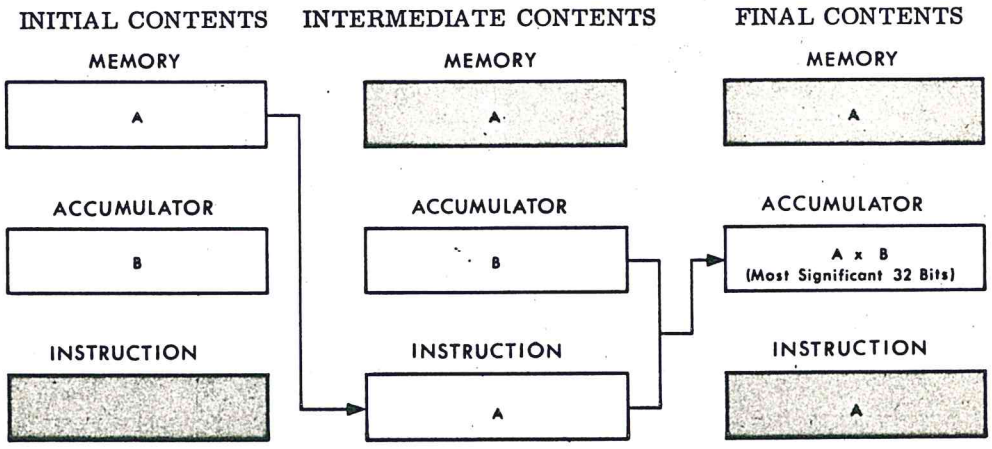
-It SHIFT 4-Bits

When t = 62, shift the contents of the Accumulator left 4 bits, inserting zeros at the right.



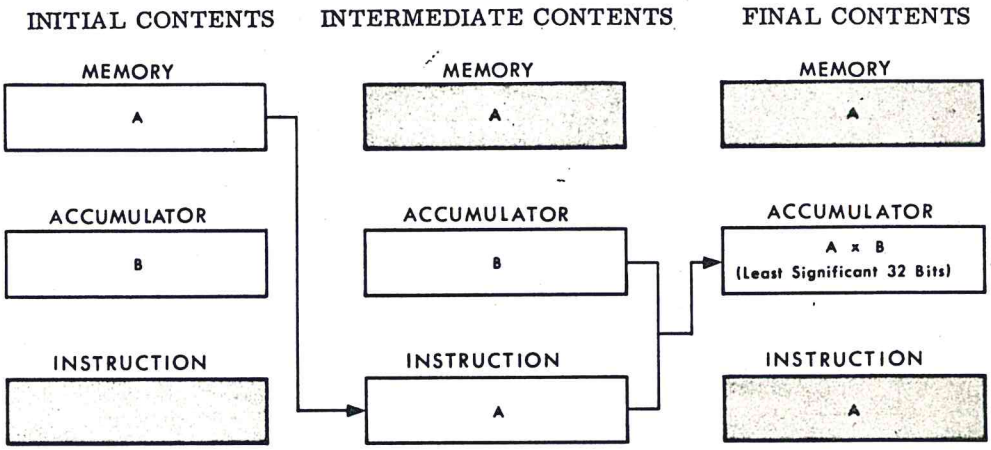
Mm MULTIPLY

Multiply the contents of the Accumulator by the contents of location m, forming a 62-bit product of which 32 bits are retained: the sign and the most significant 31 bits of the product replace the contents of the Accumulator. The Instruction Register holds the multiplier during the multiply operation.



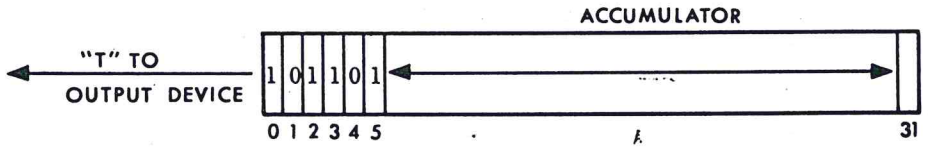
Nm MULTIPLY

Multiply the contents of the Accumulator by the contents of location m, forming a 62-bit product of which 32 bits are retained: the least significant 32 bits replace the contents of the Accumulator, occupying bit positions 0 through 31. Loss of any of the most significant bits does not cause overflow. This instruction is used mainly to accomplish left shifts. During the multiply operation, the Instruction Register holds the multiplier.



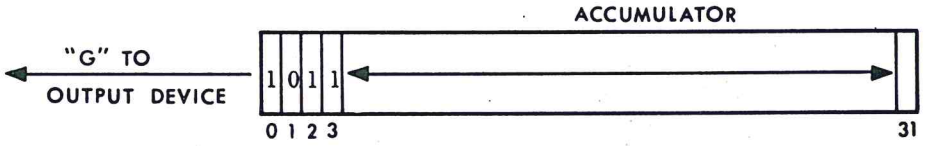
Pt PRINT 6-Bit

Transmit the character represented by bits 0 through 5 of the Accumulator to the output device specified by t. The contents of the Accumulator remain unaltered. (See Table III, Input and Output Codes.)



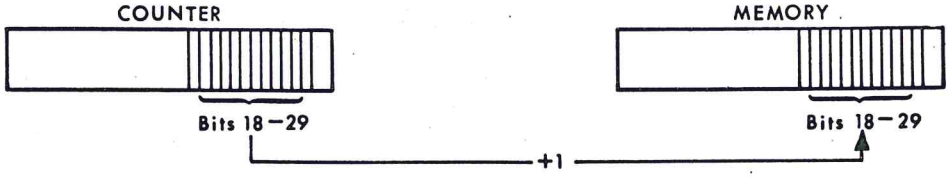
-Pt PRINT 4-Bit

Combine "1" for channel 5 and "0" for channel 6 with bits 0 through 3 from the Accumulator, then transfer this hexadecimal character to the output device specified by t. The contents of the Accumulator remains unaltered. (See Table III, Input and Output Codes.)



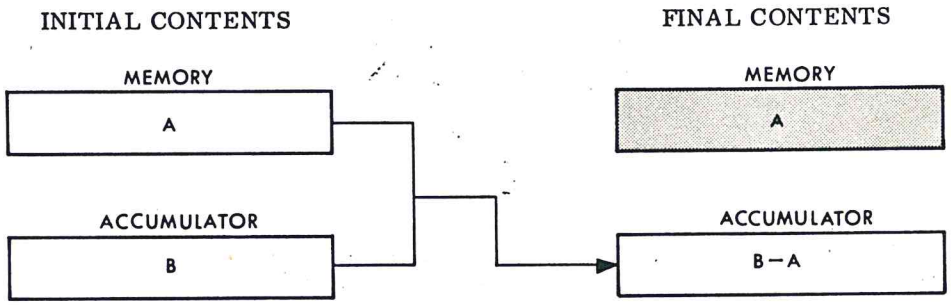
Rm SET RETURN ADDRESS

In the address portion of location m, record the address which is 2 greater than the location of the R instruction being executed (i.e., the contents of the Counter Register plus 1). The rest of the memory word remains unaltered.



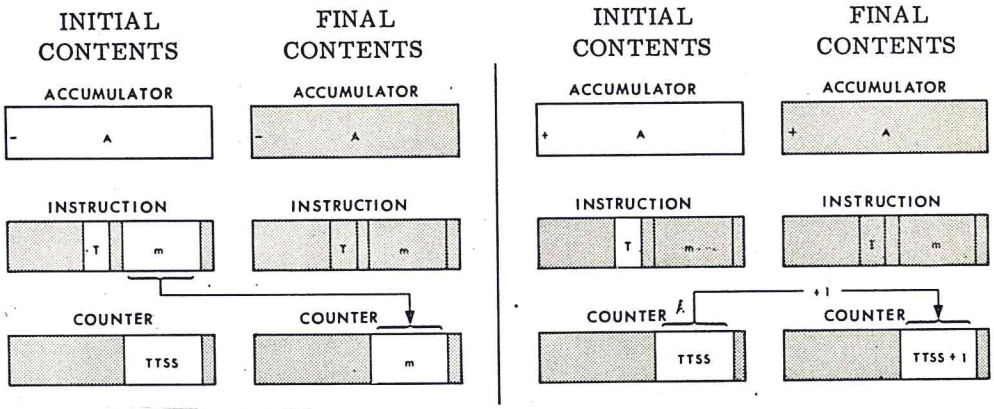
Sm SUBTRACT

Subtract the contents of location m from the contents of the Accumulator and retain the difference in the Accumulator. If a subtraction results in a number that is outside the limits of the Accumulator, overflow will occur. Memory remains unaltered.



Tm CONDITIONAL TRANSFER

If the contents of the Accumulator is negative (1 in the sign position), replace the contents of the address portion of the Counter Register with m and get the next instruction from location m. Otherwise, continue to the next instruction in sequence without altering the Counter.

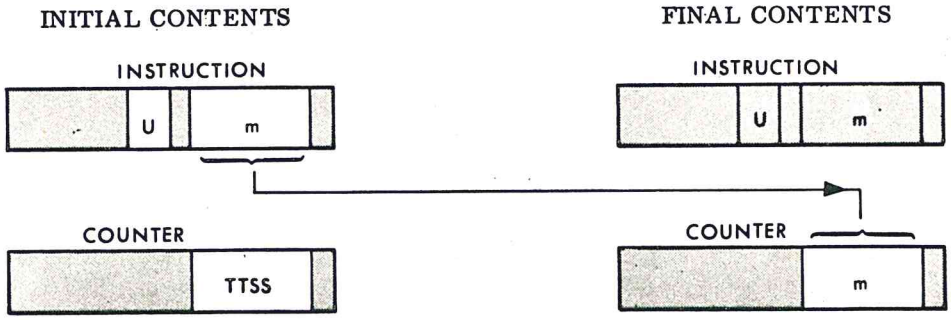


-Tm TRANSFER CONTROL

If the contents of the Accumulator is negative or if the TC switch on the console is ON, replace the contents of the address portion of the Counter Register with m and get the next instruction from location m. Otherwise, continue to the next instruction in sequence without altering the Counter.

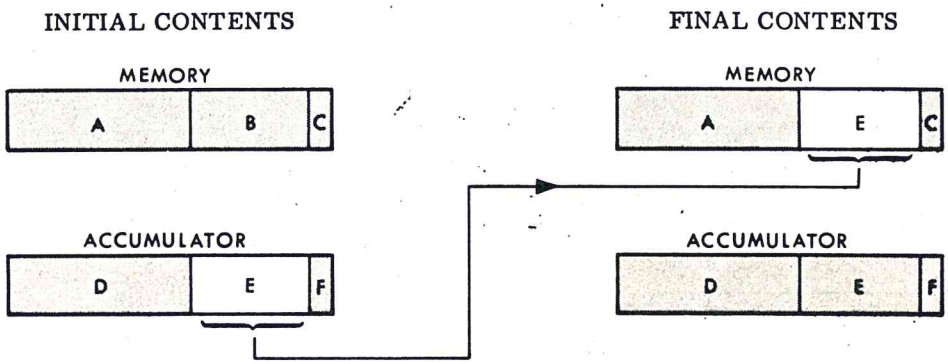
Um UNCONDITIONAL TRANSFER

Replace the contents of the address portion of the Counter Register with m and get the next instruction from location m.



Y m STORE ADDRESS

Replace the address portion of the word in location m with the address portion of the word in the Accumulator, leaving the rest of m and all of the Accumulator undisturbed.



Z t STOP

Halt computations when t = 00 or 01.

Z t SENSE BS AND TRANSFER

Interrogate the Branch Switch specified by t. If the switch is OFF, skip the next instruction in sequence. If the switch is ON, execute the next instruction in sequence. The Branch Switches are numbered 4, 8, 16, and 32. (See Sense Note below.)

-Z t SENSE OVERFLOW AND TRANSFER

If overflow is off (0 in the sign position of the Counter Register), skip the next instruction in sequence. If overflow is on (1 in the sign position of the Counter), reset the overflow bit to zero; then execute the next instruction. The track number (t) designates which, if any, Branch Switches are also to be interrogated. If Sense Overflow is combined with Stop (800Z0000), the skip or no skip is deferred until after the stop. If no Branch Switches are to be tested and no stop is desired, the track can be 02 or 03. (See Sense Note below.)

Sense Note: Overflow and/or any combination of Branch Switches can be interrogated with one Sense and Transfer instruction. If any are OFF, the next instruction will be skipped. If all are ON, the next instruction will be executed.

TIMING AND OPTIMIZING

Sector Reference Timing Track

In the LGP-21 all instructions are executed in sequence. The time required for completing a specific operation depends, in part, on the location in memory of the instruction and of its operand, if one is necessary. The process by which the computer obtains and executes an instruction is called an instruction cycle. An instruction cycle begins with a memory search for the instruction word and ends with the commencement of the search for the next instruction word.

The complete cycle consists of four phases:

Phase 1 - Search for the instruction.
Phase 2 - Transfer the instruction from main memory to the Instruction Register and increment the Counter Register by 1.

Phase 3 - Search for the operand.
Phase 4 - Execute the instruction.

In order for the computer to find a specific location in memory, a Sector Reference Timing Track is used. This track contains the sector numbers 00 through 127 permanently pre-recorded at the time of manufacture. As explained under "MEMORY," each of the concentric circles on the disc contains 128 sectors. Sector addresses are numbered 00 through 63 for programming purposes. Therefore, on the Sector Reference Timing Track numbers greater than 63 are interpreted as modulo 64. For example, sector 97 is sector 33 (i.e., 97 - 64 = 33) for all odd-numbered tracks.

The Sector Reference Timing Track has only a read head and cannot be modified by the programmer. The numbers on this track pass under its read head one sector before the corresponding sector in main memory passes under its read head. Thus, when a specified sector address is read on the Sector Reference Timing Track, the read/write head on the appropriate track is activated, and the word can be read from or recorded in memory. For example, assume the contents of Location 1432 is to be brought to the Accumulator. When the Sector Reference Timing Track reads 32, read head 14 is activated, and as sector 32 moves under that read head, its contents is copied into the Accumulator. See Figure 5.

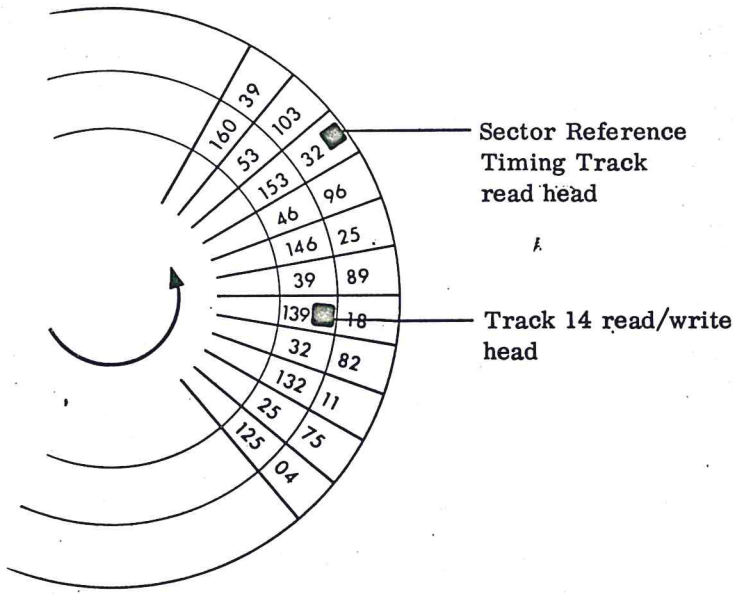


FIGURE 5 — Sector Reference Timing Track

This may be more easily understood if two instructions are considered in sequence. Assume that the instruction B4458 is stored in memory Location 1115, and the instruction A4452 is in Location 1116. When executed, these instructions will result in some value—say 8—being brought to the Accumulator from 4458 and another value—say 7—being added to it.

During Phase 1 the Counter Register contains the address 1115, so the computer searches the Sector Reference Timing Track for sector 79 (79 - 64 = 15). When it is read, the read head on track 11 is activated, and Phase 1 ends. (Figure 6)

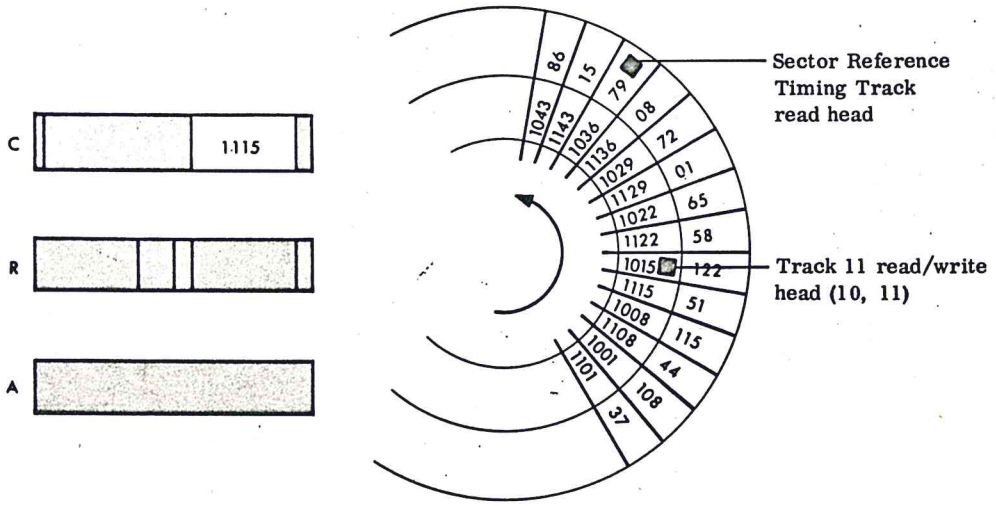


FIGURE 6 — Instruction Cycle - Phase 1

In Phase 2 the contents of Location 1115 is read into the Instruction Register, and the Counter Register is incremented by 1, so that it now contains 1116. (Figure 7).

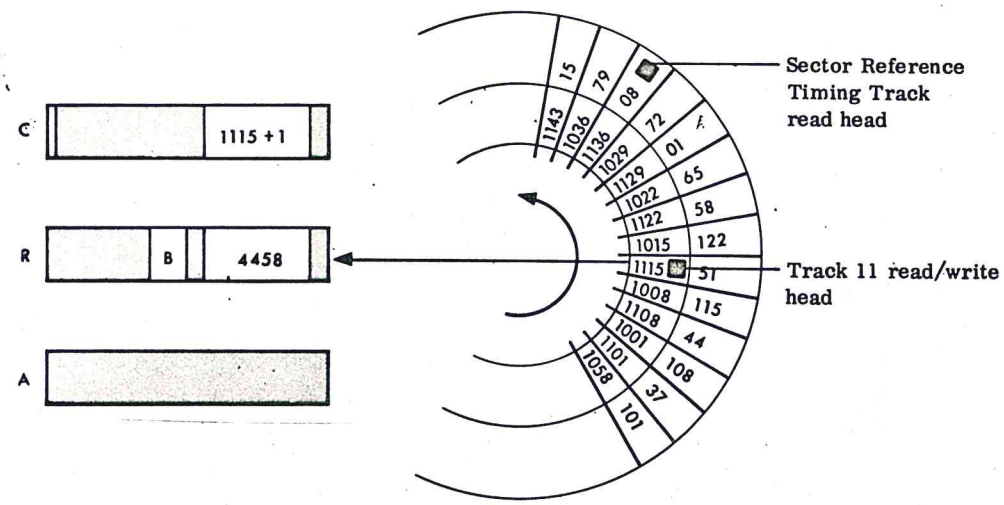


FIGURE 7 — Instruction Cycle - Phase 2

During Phase 3 the computer searches the Sector Reference Timing Track for the sector specified in the Instruction Register—that is, sector 58. (Figure 8).

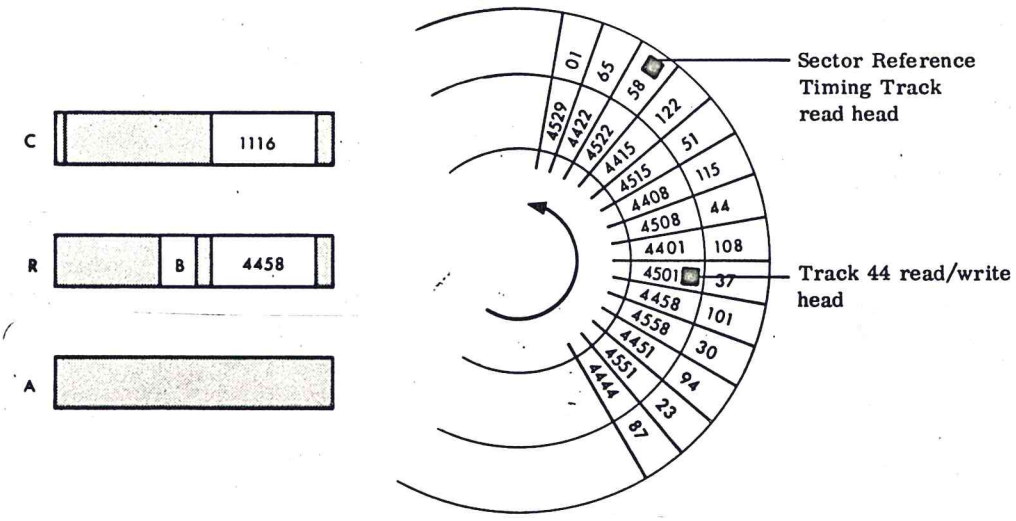


FIGURE 8 — Instruction Cycle - Phase 3

When sector 58 is read, Phase 3 ends, and the computer goes to Phase 4 to execute the instruction B4458. Therefore, the contents of Location 4458 (the number 8) is copied into the Accumulator. (Figure 9).

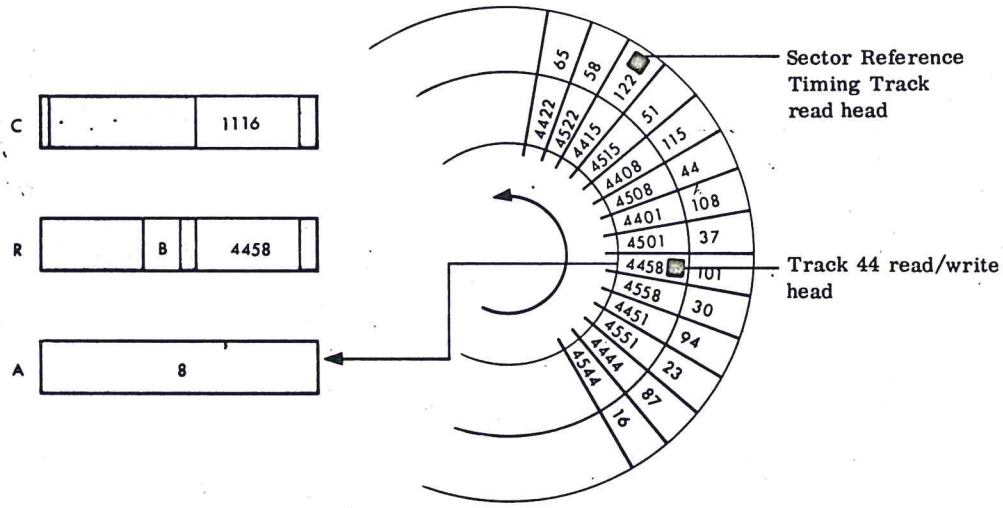


FIGURE 9 — Instruction Cycle - Phase 4

Then the cycle begins again:

Phase	Activity
1	Counter Register contains 1116, so search for sector 80 on the Sector Reference Timing Track. When sector 80 is found, activate the read head for Track 11.
2	Copy contents of Location 1116 (A4452) into the Instruction Register. Increment Counter Register to 1117.

3 Search for sector 52. When it is read, activate the read head for Track 44.

4 Execute the instruction; that is, add the contents of 4452 (the number 7) to the contents of the Accumulator (8) and leave the sum (15) in the Accumulator.

Note: When a Sense and Transfer instruction results in a "skipped" instruction, the instruction is actually brought into the Instruction Register, but is not executed. That is, Phases 3 and 4 of the skipped instruction are bypassed, and the computer advances directly to Phase 1 of the following instruction.

Timing

Generally, if all four phases of an instruction can be executed before the disc turns past the location of the next instruction in sequence, the instruction is said to be optimum. However, there are a few instructions which require more time for their operations than the four phases allow. These exceptions include the multiply, divide, input, and output operations.

During Phases 1 and 3 the computer searches for the specified sector and then activates the appropriate read/write head. Either of these phases can require one or more word-times. Phase 2 is always one word-time. Phase 4 requires one word-time for all instructions except M Multiply, N Multiply, and Divide. These three (N, M, and D) require 63, 65, and 66 word-times respectively.

Optimization

Figure 10 shows a device which is useful in determining the optimum sector for the operand of any instruction. For example, if an Add instruction is stored in

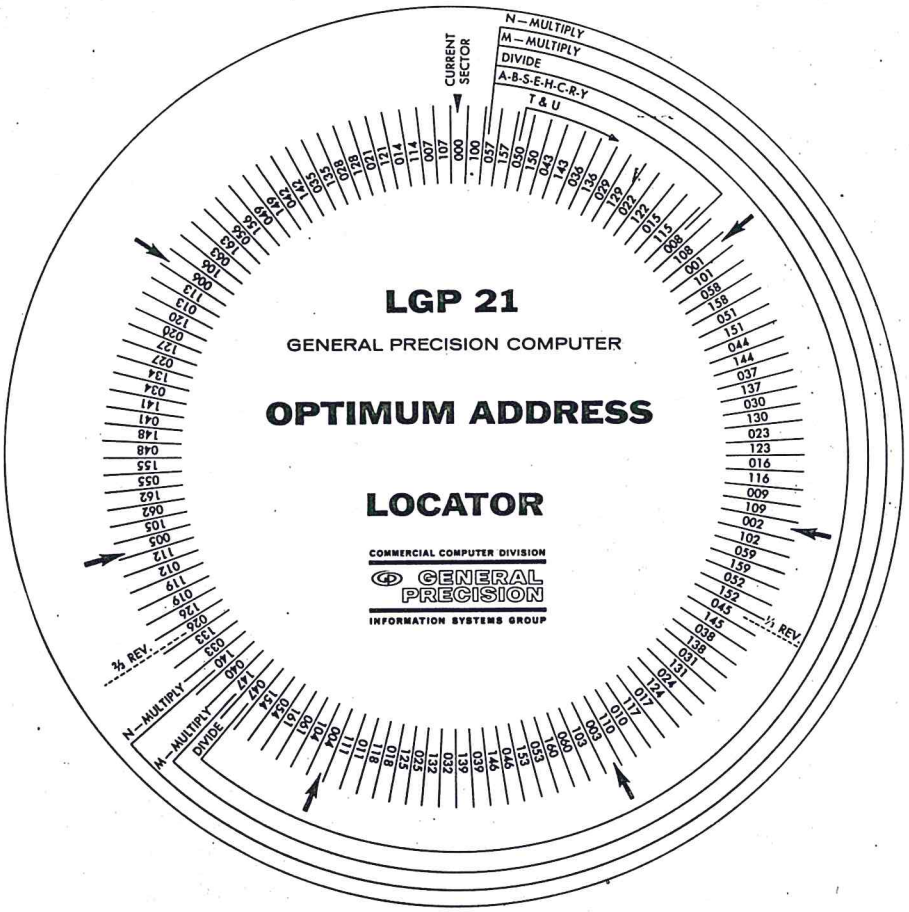


FIGURE 10 — Optimum Address Locator

sector 00 of a track, it is optimum when it can be executed before sector 01 passes under the read head. By referring to Figure 10 it can be seen that for an optimum Add instruction in sector 00 of an even-numbered track, its operand must be in one of the following sectors: 57, 50, 43, 36, 29, 22, or 15 on an odd-numbered track (indicated on the wheel by the initial digit "1"), or 57, 50, 43, 36, 29, 22, 15, or 08 on an even-numbered track (indicated by the initial digit "0").

Figure 11 shows the LGP-21 commands and the optimum operand addresses for an instruction in an even-numbered track, sector 00.

Instruction in Location 000	Optimum Operand Addresses	Distance from Instruction location to Optimum Operand (in word-times)
Bring, Add, Subtract, Hold, Clear, Extract, Set Return Address, Store Address	057, 157, 050, 150, 043, 143, 036, 136, 029, 129, 022, 122, 015, 115, 008	2 through 16
N-Multiply	057, 157, 050, 150, 043, ... 040, 140	2 through 81
M-Multiply	057, 157, 050, 150, 043, ... 047, 147	2 through 79
D-Divide	057, 157, 050, 150, 043, ... 154, 047	2 through 78
Unconditional Transfer, Conditional Transfer	050, etc.	4 or more
Others	unrelated	unrelated

FIGURE 11 — Optimum Operand Addresses

Depending on whether an instruction is optimized or not, certain time intervals are required for the computer to read an instruction, execute it, and be ready to read the next instruction. Figure 12 shows the varying timing requirements:

Instruction	Time in Milliseconds	
	Optimum	Non-optimum
Bring, Add, Subtract, Hold, Clear, Extract, Set Return Address, Store Address, Input Shift	7.26	58.11
N-Multiply, M-Multiply, D-Divide	58.11	108.96
Unconditional Transfer, Conditional Transfer	1.60	Each sector beyond optimum adds .40
Sense	7.26 or 14.52	

FIGURE 12 — Optimum Timing

Input/Output Timing

An input instruction will be delayed within its cycle until a start signal is received from the input device. Three word-times plus the Phase 1 search, plus the time required for reading or typing determine the total time for any input instruction.

Print instructions should be timed at least 2 revolutions apart for the 121 Tape Typewriter or 1/3 revolution apart for the 151 Tape Punch if they are to operate at their rated speeds. An output operation will not delay the computer unless the selected device is already in use. For example, if an output to the tape typewriter is followed by an output to the 151 Tape Punch, the computer will not delay on the second output instruction even though the tape typewriter is still busy. If the first and second output instructions both select the tape typewriter, the computer will delay on the second instruction until the typewriter is ready.

COMPUTER CONTROL PANEL

Operational control of the computer is effected through the control panel switches, all of which are clearly identified by function or related action. See Figure 13.

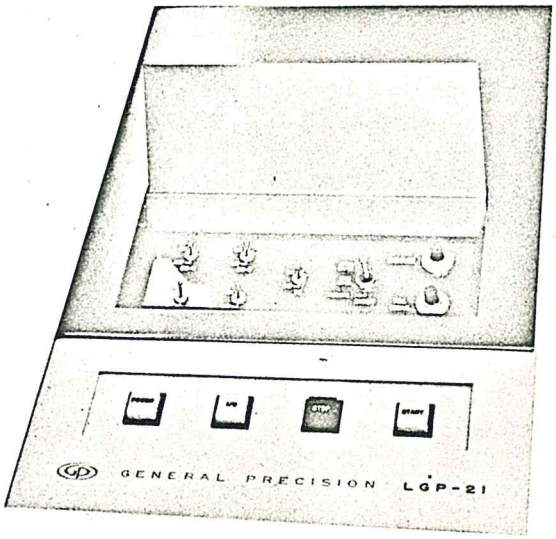


FIGURE 13 — Computer Control Panel

MODE
This is a three-position toggle switch:

NORMAL - When the MODE switch is set to this position, the computer executes instructions at high speed. When the START switch is depressed, the execution of instructions will begin, commencing with the instruction whose address is contained in the Counter.

ONE OPERATION - If the computer is operating in Normal mode and the MODE switch is moved to ONE OPERATION, the computer will stop after the next Phase 4, the execute phase. If the computer is stopped in One Operation mode, depressing the START switch will start the computer cycling through the instruction whose address is in the Counter Register, and computation will stop after the execute phase for that instruction. The EXECUTE switch is operative only in One Operation mode. Going from Manual Input mode to One Operation mode will de-select the tape typewriter.

MANUAL INPUT - This position sets the Accumulator to receive input. It also selects the typewriter for 4-bit input, but does not de-select other devices. If other devices are selected, the I/O switch should be depressed, or information may not enter correctly. All typed characters enter the Accumulator. No instruction can be executed in Manual Input mode since the START switch is inoperative.

FILL CLEAR
FILL CLEAR is a momentary switch which transfers the contents of the Accumulator to the Instruction Register and resets the Counter Register to zero. This switch is inoperative in Normal mode.

EXECUTE
This momentary switch causes the instruction in the Instruction Register to be executed. It is operative only in One Operation mode.

Transfer Control

The TC switch can be set ON or OFF. This switch is used in conjunction with the negative T (Conditional Transfer) command. A negative T instruction will cause the computer to get the next instruction from the location designated by the operand address if the contents of the Accumulator tests negative or if the TC switch is ON, otherwise it causes the computer to continue to the next instruction in sequence.

Branch Switches

The four branch switches are labeled BS-32, BS-16, BS-8, and BS-4. Each is a two-position switch which is set ON or OFF. These switches are used in conjunction with the Z (Sense and Transfer) command. A Z instruction whose track-address corresponds to one or more of the branch switches will cause the computer to skip the next instruction if any designated switches are OFF, or to execute the next instruction if all designated switches are ON.

POWER

This switch turns power ON or OFF. Power for all units in the system is in series with this switch. Any units that are previously set ON will have their power turned ON as the switch is depressed. About thirty seconds after power is turned ON, the switch will light to indicate the machine has attained full power.

I/O

I/O is a momentary switch which clears the Accumulator and de-selects all input and output devices. If the computer is in Manual Input mode, I/O will not de-select the typewriter. The switch is lighted and operative during input and output and when the computer is in Manual Input mode.

STOP

This indicator lamp lights immediately when the computer is turned ON, and is lit whenever the computer is not executing instructions.

START

START is a momentary switch which causes the computer to execute the instruction specified by the Counter Register. In Normal mode this will begin the full-speed execution of instructions. In One Operation mode, only one instruction will be executed. The switch is not operative in Manual Input mode. The light beneath the switch is ON whenever the computer is operating.

In addition to those on the control panel, there are two toggle switches on back of the computer:

INTERLOCK

The LGP-21 has a circuit breaker to interrupt operation if the air-flow from the fan becomes blocked. This interruption stops computer operation to prevent overheating. Following such an interruption, the condition that caused it should be corrected; then the circuit may be reset by moving the INTERLOCK switch from the up position down and up again. It should be noted that, depending upon the operation in effect when the interlock occurred, information stored in memory may have been destroyed and may have to be re-entered.

WRITE ENABLE

This switch may be set ON or OFF. When it is ON, reading from and recording in all sectors of all tracks may occur. When it is set to OFF, 1024 words—specifically Tracks 00 through 15—are protected; that is, information may be transferred from any word within this area to the Instruction Register or the Accumulator, but no information can be recorded in any word in this area. This

feature allows the operator to lock a program in memory so that it cannot be destroyed inadvertently.

INPUT/OUTPUT UNIT

The primary input/output unit for the LGP-21 is the Model 121 Tape Typewriter. In addition to a standard typewriter keyboard, the unit has a paper-tape punch, paper-tape reader, and various levers for controlling their operations. See Figure 14.

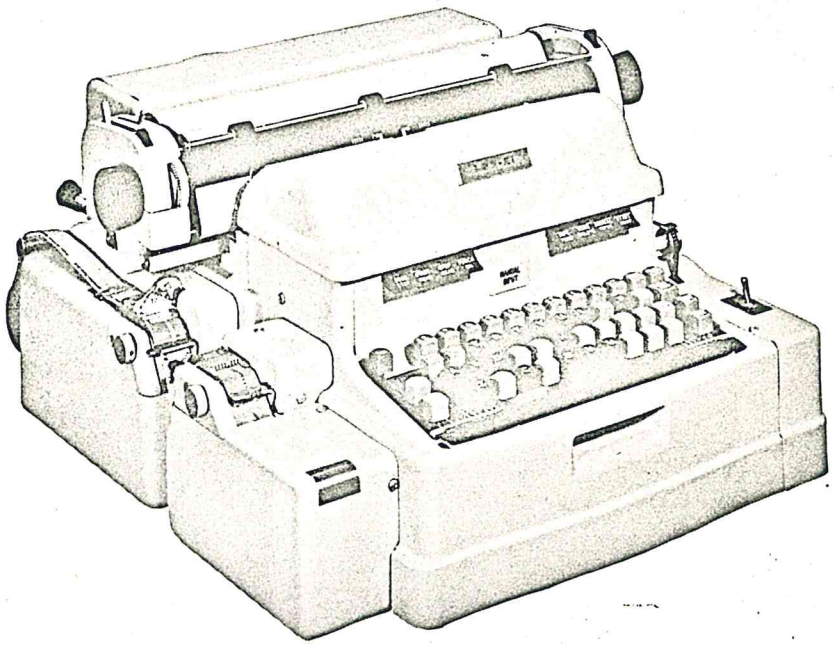


FIGURE 14 — Model 121 Tape Typewriter

POWER ON-OFF
This switch, in the lower right-hand corner adjacent to the keyboard, sets the typewriter so that power will be turned ON or OFF when the computer power is ON. The carriage is interlocked and should not be moved when power is OFF.

START COMP
When the computer has selected the typewriter for input, the START COMP lever terminates input and allows the computer to proceed to the next instruction. The START COMP lever will stop the paper-tape reader whenever it is running on-line or off-line. The functions of the STOP READ lever are identical to the START COMP lever.

MANUAL INPUT
If this lever is down and the typewriter is selected for input, information can be transmitted to the computer from the keyboard only. If this lever is raised, information is received from the tape reader when the typewriter is selected for input.

CODE DELETE
Operative only when the PUNCH ON lever is depressed, this lever is used to delete an error in the tape by punching holes in channels 1 through 6. The tape must be manually backspaced one character to delete the error. By holding down TAPE FEED and CODE DELETE at the same time, a series of delete codes can be punched.

TAPE FEED
This lever feeds tape into the punch, which then punches only sprocket feed holes. TAPE FEED is operative only when PUNCH ON is depressed.

Manual Input Light
This light is illuminated when the typewriter is selected for input to the computer and the MANUAL INPUT lever is down.

PUNCH ON
The PUNCH ON lever turns the tape punch ON, allowing any character typed from the keyboard or read from the tape reader to be punched. TAPE FEED and CODE DELETE are operative only when PUNCH ON is depressed. Raising the lever turns the punch OFF.

STOP READ
Used interchangeably with START COMP.

START READ
This lever starts the tape reader. Reading will continue until a Conditional Stop Code is read, providing the COND STOP lever is raised; or until the STOP READ or START COMP lever is depressed.

COND STOP
This lever, when depressed, allows the tape reader to read without being stopped by the Conditional Stop codes. This lever must be raised during input to the computer from the tape reader.

Paper Guide
Located just to the rear of the platen, this guide should be adjusted horizontally so that it just touches the left edge of the paper form.

Tab Stop
Under the cover to which the paper guide is attached is the tab rack numbered 8 through 136 in increments of 4. A tab stop is a metal positioner that can be inserted in any notch along the tab rack. When the TAB key is depressed or the Tab code is read, the carriage will move to the next position containing a tab stop.

Left Margin Stop
In front of the tab rack is the margin rack numbered 0 through 68 in increments of 4. The margin stop is the sliding assembly mounted on the margin rack. To move this assembly, press down on its center and slide it along the rack. The right end of the stop is the indicator. The setting of the margin stop determines the left margin position.

Automatic Carriage Return
Behind the tab rack is a carriage return plate. An automatic carriage return positioner can be placed anywhere along the plate. An automatic return occurs when the carriage reaches this return positioner as the result of a tab jump; i.e., because the Tab key is depressed, a Tab code is read from tape, or the computer outputs a Tab code. If this positioner is reached as a result of single-

character steps, the typewriter may jam. This condition may be cleared by striking the Carriage Return key manually. However, any input or output that occurred at the time of the jamming may be invalid.

Paper Scale
The paper scale is printed on the metal shield in front of the platen. By viewing the paper scale through the type guide, one can determine the exact position of the carriage and exactly where characters will print.

Type Guide
This guide indicates the position of the carriage and the location where the characters will print.

Writing Line Finder
The bottom of the typed line will be exactly above the top edge of the writing line finder. It is used to align a previously typed page in the platen for additional typing.

Paper Release
The paper release lever is located at the top left-hand corner of the moveable carriage assembly. When this lever is pulled forward, the paper can be straightened or removed.

Line Spacer
To the right of the paper release lever is a lever which permits selection of single, one and one-half, or double spacing between lines.

Platen
The roller, around which paper is inserted and against which the type bars strike, is called the platen.

Carriage Release (right and left)
There are two Carriage Release buttons, one located to the right and one to the left of the platen. When either or both are held down, the entire carriage assembly can be freely moved right or left. The carriage should not be moved when power is off.

Platen Knobs (right and left)
The platen knobs, located at each end of the platen, are used for turning the platen forward or backward.

Platen Variable
When this button, located in the center of the left platen knob, is depressed, the platen is released to allow the operator to position the paper at other than standard line spacing. Releasing the button restores standard line spacing.

Margin Release
This lever, which is located behind the left platen knob, can be raised to move the carriage to the left of the margin stop.

Ribbon Positioner
The ribbon position lever, located on the right side of the typewriter below the carriage, positions the ribbon for typing through its upper or lower part, or for typing stencils.

COND STOP (')
This key is used to punch a Conditional Stop code (') into paper tape. When sensed by the tape reader, this code stops the reader and sends a start signal

to the computer.

TAB
This key moves the carriage to the next established tab position.

COLOR SHIFT
This key shifts and locks the ribbon for typing through its upper or lower half.

CAR RET
This key returns the carriage to the left margin and spaces the paper to the next typing line.

BACK SPACE
This key moves the carriage back one letter space.

Space
This bar moves the carriage forward one letter space.

LOWER CASE, UPPER CASE
These keys lock the keyboard in position for typing lower or upper case characters.

TAPE INTERLOCK
Both the reader and punch contain a tape interlock that stops the device if the tape breaks or if the supply is exhausted.

FEED KNOBS (Reader and Punch)
The reader and punch feed knobs are located on the left of the read and punch heads, respectively. These knobs can be used to move the tape forward or backward manually.

OPTIONAL EQUIPMENT

Model 101 Visual Oscilloscope Display

The Visual Oscilloscope Display is a separate unit consisting of an oscilloscope and the controls necessary to adjust the images displayed on it.

The oscilloscope furnishes the operator with a visual representation in binary form of the content of the three control registers: Counter, Instruction, and Accumulator.

The Counter Register displays the address of the next instruction to be executed and an indication if overflow has occurred since the last overflow condition interrogation. A "1" in the sign position of this register indicates that overflow has occurred; a "0" that it has not.

The Instruction Register displays the last instruction executed, or the second operand, in the case of multiplication and division.

The Accumulator displays the results of the last computation or data manipulation. See Figure 15.

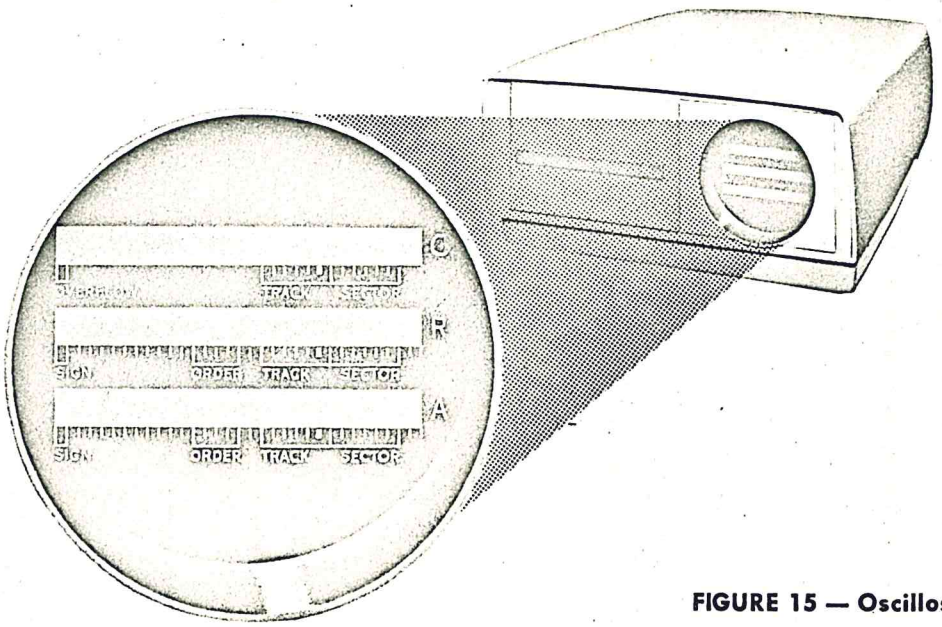


FIGURE 15 — Oscilloscope

On the left side of the oscilloscope are controls for adjusting the images of the respective control registers (Figure 16).

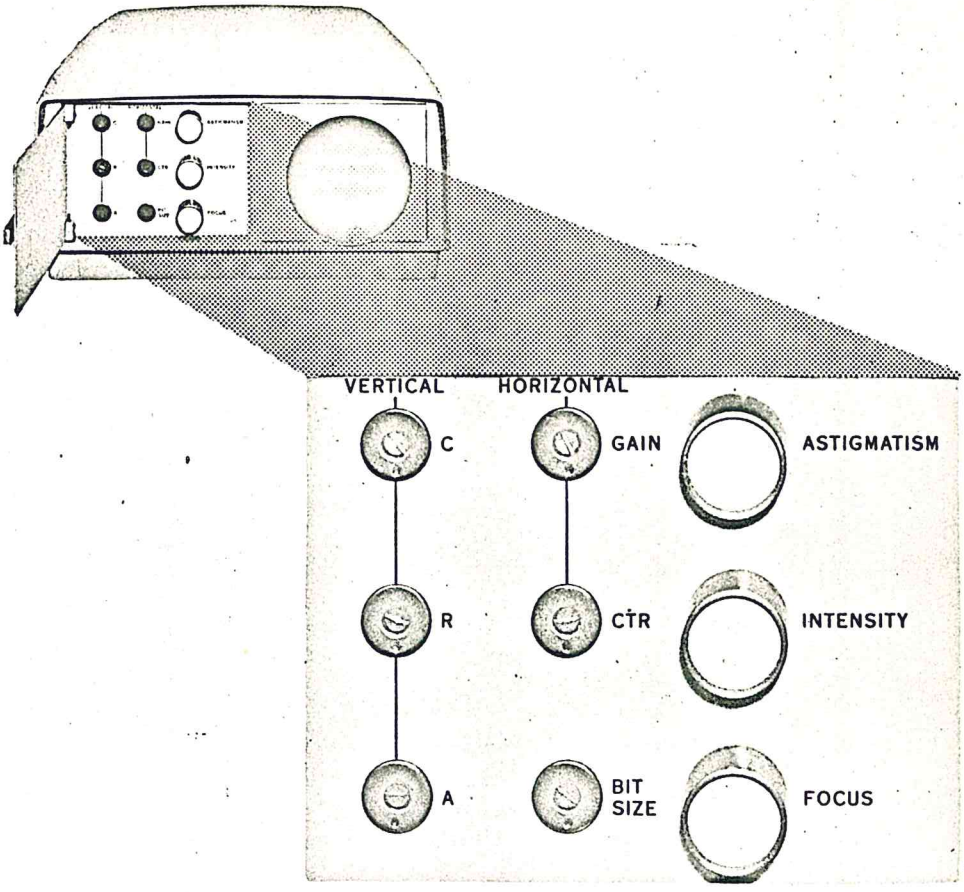


FIGURE 16 — Oscilloscope Controls

Adjustments are possible for each register by turning the appropriate screw under the designations HORIZONTAL or VERTICAL. The screws are labeled C for Counter Register, R for Instruction Register, and A for Accumulator. By turning a screw under VERTICAL, the operator can adjust the vertical dis-

placement of the designated register. Beside each of the screws in the HORIZONTAL row are labels specifying the kind of adjustment that can be effected by turning the particular screw: GAIN increases or decreases the width of the bit patterns, CTR centers the display in the windows, and BIT SIZE increases or decreases the amplitude of the bits displayed. Each of these screws affects all three register displays. The three knobs are also labeled to indicate their functions: ASTIGMATISM, INTENSITY, and FOCUS. ASTIGMATISM and FOCUS are used together to adjust the sharpness of the trace, and INTENSITY is used to make the image more or less brilliant.

Model 141 Paper-Tape Reader

The Model 141 Paper-Tape Reader is a self-contained, asynchronous device for reading any standard 5 to 8 channel perforated tape. Its reading speed is rated up to 60 characters-per-second. Tape can move forward or in reverse. Tape wear is exceptionally low, and standard paper-tapes may be used hundreds of times. See Figure 17.

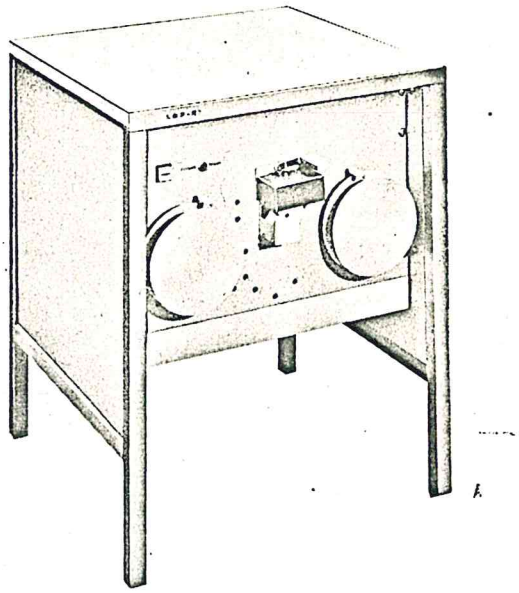


FIGURE 17 — Model 141 Paper-Tape Reader

The tape transporting equipment consists of two reels, mounted one on each side of the read head. They are rotated by a gear and brake mechanism actuated by tape tension arms. Either reel can be the take-up or supply reel, depending upon the direction of tape movement.

The Reader is controlled by two switches: a button-type POWER switch and a toggle switch for positioning the tape. The unit may be turned ON by depressing the POWER switch. Depressing the switch a second time turns the unit OFF. This switch is lighted while the unit is ON. The toggle switch is a momentary one which controls the bi-directional movement of the tape. By holding this switch in the direction the tape is to move, the operator can position a tape in the read head. Information enters the Accumulator of the computer only when the tape is moving forward (i.e., right to left). Tapes may be rewound at speeds up to 300 characters-per-second.

Model 151 Paper-Tape Punch

The Model 151 Paper-Tape Punch is a self-contained asynchronous unit capable of perforating paper-tape at speeds up to 60 characters-per-second. It is equipped with two reels: a supply reel, mounted behind the right side of the panel,

and a take-up reel, mounted on the left front-side of the panel. The take-up reel is rotated by a gear and brake mechanism activated by the tape tension arm. See Figure 18.

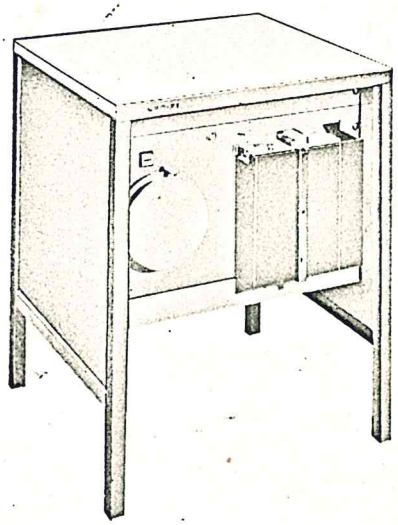


FIGURE 18 — Model 151 Paper-Tape Punch

The punch is controlled by two button-type switches: a POWER switch and a tape feed switch. The POWER switch is a momentary switch which is depressed to turn the power ON; a second depression turns it OFF. The switch is lighted when the unit is ON. The tape feed switch is also a momentary switch. When it is depressed and held, tape is fed to the punch head which punches sprocket (feed) holes only.